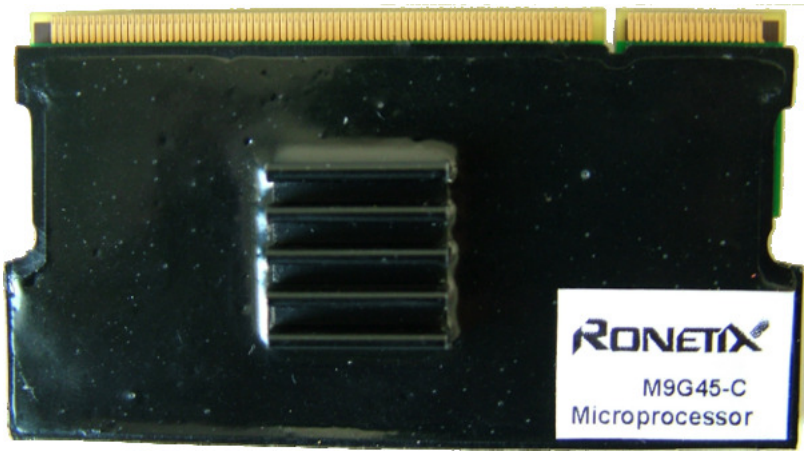
M9G45-C Microprocessor

M9G45-C Microprocessor v1.2 and v1.3
Data Sheet



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DEVELOPMENT TOOLS

Acknowledgement

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Acknowledgments:

Contents

Change log

June 2011	- fix WKUP and SHDN signals description - add Debug Unit description - add RoHC statement - table with not populated elements - e-mail for order and request
January 2011	- SO-DIMM signal clarifications. - Add module versions. - correct a type AT92SAM9G45 to AT91SAM9G45
November 2010	- USB Device and Host Port(High Speed) compatibility.
October 2010	- USB Device Port(Data+ signal) compatibility.
September 2010	- Initial release.

1 Features

- Microprocessor

  CPU Main

  - 400MHz ARM926EJ-S ARM Thumb Processor
  - 32 KBytes Data Cache, 32 KBytes Instruction Cache, MMU

  Peripherals

  - LCD controller
  - UTI-R BT. 601/656 Image Sensor interface
  - USB High Speed OTG(Host and Device), USB Full Speed Host
  - 10/100 Mbps Ethernet MAC Controller
  - Two High Speed Memory Card Hosts (SDIO, SDCard, MMC)
  - AC'97 controller
  - Two Master/Slave SPI
  - 10-channels 10-bit ADC with 4-wire Touch Screen support
  - Four USARTs
  - Two Three-channel 16-bit Timer/Counters
  - Two Synchronous Serial Controllers (I2S mode)
  - Four-channel 16-bit PWM Controller
  - Two Two-wire Interfaces

  System

  - Backup section for power down and/or slow clock power saver.
  - Selectable 32768 Hz Low-power and 12 MHz Crystal Oscillators
  - Advanced Interrupt Controller
  - Debug Unit with UART
  - 37 DMA Channels
  - Two Programmable External Clock Signals

  I/O

  - Five IO controllers with 32 input/output lines each.
  - 160 Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os with Schmitt trigger input

  Package

  - 324-ball TFBGA, pitch 0.8 mm

- 128MiB DDR2 SDRAM for system and video ram
- 256MiB NAND flash
- DS2401 48bits SN on 1-Wire Dallas protocol
- 4MiB or 8MiB DataFlash(optional)
- 10/100 Mbps Ethernet PHY
- Single power supply +3.3V
- Power backup rail
- Power enable, wake up and shutdown pins
- SO-DIMM 200 (JEDEC MO-224) connector
- Outline DIMM per JEDEC MO-224
- Software

- AT91Bootstrap 2.13
- U-Boot 2010.06
- Linux Kernel 2.6.30
- OpenEmbedded distribution KaeilOS
- Windows CE 6.0 R3

2 Description

2.1 CPU

The ARM926EJ-S implements ARM architecture version 5TEJ and is targeted at multitasking applications where full memory management, high performance. The ARM926EJ-S processor supports the 32-bit ARM and 16-bit THUMB instruction sets, enabling the user to trade off between high performance and high code density.

The support of 8 bits Java bytecodes provides the ability of running variety of Java applications.

2.2 Memories

2.2.1 DDR2 SDRAM

Two DDR2 SDRAM chips with capacity of 128MiB for program and vide memory. The chip is powered with 1.8V, clocked at 133MHz and transfer data and commands through 16 bits data bus. Video and operating memory share the same chips. Video memory and bandwidth usage is shown on Table 2 LCD displays .

The memory is on EBI DDR2 interface and ran by DDR_CS0 signal.

2.2.2 NAND

The NAND flash provides power nonvolatile memory storage. Its memory capacity allows storage of completely functional embedded operating system with GUI, like GNU/Linux and Windows CE. You can divide a part of NAND for custom data storage or use the operating system file system to write/read and change files.

The NAND chip is with capacity of 256MiB and transfer data through 8 bits data bus. Attached to External Bus Interface and selected by CS3 signal. Chip is powered with 3.3V.

2.2.3 DataFlash

The DataFlash is on SPI0 controller and is enabled with SPI0_NCS0. This is an optional component, and could have 4MiB or 8MiB capacity.

DataFlash succeed the EEPROM with making reliable and easy to use memory interface. It is intended for special storage like a calibration data or parameter tables. Get in contact with Ronetix to set this option.

2.3 Clock sources

Three clock sources provides the work power of the module. The main MCU oscillator is used to clock the at its higher performance, but when power consumption is required the MCU could be clocked with slow clock. The Ethernet transceiver is clocked with dedicated oscillator which could be disabled with PIO port D pin 2 if no Ethernet is needed and low power consumption is required.

- one 12MHz XTAL for MCU main oscillator.
- one 32.768KHz XTAL for MCU slow oscillator.
- one 50MHz crystal clock oscillator for the Ethernet PHY. The oscillator can be enabled or disabled with PIO port D pin 2.

2.4 Power supply

The module should be powered with +3.3V. In case of backup power is needed then on the VBAT line uninterruptible power source could be applied. The VBAT maximum power voltage is 4V(check AT91SAM9G45 electrical characteristics).

The required 1.8V and 1.0V powers are made by on-board DC-DC converters. The converters enable pin is on the SO-DIMM connector.

The ethernet PHY provides separate GND_BG and 3V_ETH power supply lines for the transformer. More at subsubsection 3.2.1 Ethernet signals .

The MCU could be shuted down by software when writing to a register in the Shutdown Controller, which then activates the SHDN(shutdown) output pin to switch off the power sources, but the back-up power must remain if later the wake up signal is going to be used.

The provided wake up input can brings the system running.

2.5 On-board peripherals

2.5.1 Serial number chip

The module has a serial number chip DS2401. It can be used generate unique MAC Ethernet address or identification. The serial number pin is connected to MCU's PA31 as well on the SO-DIMM connector for external access.

2.5.2 Ethernet PHY

The integrated MAC controller and the on-board PHY transceiver reduces the needed external components to a 10/100 Ethernet magnetic trafo and RJ-45 socket.

Table 1: PHY chips

PHY chip	board version	output analog power supply
DP83848I	v1.2	3.3V
DM9161A	v1.3	2.5V
DM9161B	v1.3	1.8V

DM9161B has a power save mode compared to DM9161A.
DM9161BI like DM9161B but supports Industrial-grade: -40℃ to +85℃.

2.6 MCU peripherals

2.6.1 USARTs

The Universal Synchronous Asynchronous Receiver Transmitter (USART) provides one full duplex universal synchronous asynchronous serial link. It can operate in RS-232 and RS-485, and ISO7816 T = 0 or T = 1 smart card slots and infrared transceivers. It also has remote loopback, local loopback and automatic echo test modes.

The four USARTs are available on the SO-DIMM connector.

2.6.2 Debug Unit

The Debug Unit provides a single entry point from the processor for access to all the debug capabilities of Atmel's ARM-based systems using JTAG emulator.

The Debug Unit also makes the Debug Communication Channel (DCC) signals provided by the In-circuit Emulator of the ARM processor visible to the software

Debug Unit pins are available on the SO-DIMM connector. The Debug Unit UART implemented features are 100% compatible with the standard Atmel USART

2.6.3 USB

There are two USB Host Ports - full speed OHCI and High speed EHCI, and one USB Device High speed port. USB Host Port A is directly connected to the first UTMI transceiver. The Host Port B is multiplexed with the USB device High speed and connected to the second UTMI port. The selection between Host Port B and USB device high speed is controlled by the UDPHS enable bit located in the UDPHS_CTRL control register.

Multiplexing Host and Device through UTMI allows to create and USB On-The-Go device. Choose one free PIO pin on the SO-DIMM to act as USB OTG ID pin. The cable sets the initial role of the connected USB devices, the grounded ID pin sets initially the MCU to host.

2.6.4 PIO

The AT91SAM9G45 features 5 PIO controllers, PIOA, PIOB, PIOC, PIOD and PIOE, which multiplexes the I/O lines of the peripheral set.

The PIO lines can be used for driving leds, and reading button status. The PIO can act on signal level or signal transition with triggering interrupt.

The signals on the SO-DIMM pins are multiplexed. This means that some devices can not be used at the same time. Take a look at Table 4 Signal description of the multiplexed signals and devices.

2.6.5 LCD Controller

The LCD controller embedded in AT91SAM9G45 supports single and dual scan color and monochrome passive STN LCD panels and single scan active TFT LCD panels. The maximal resolution supported is up to 2048 x 2048.

Combining Touch Screen ADC Controller and the LCD Controller a graphical keyboardless systems can be designed.

The Table 2 LCD displays shows some used displays and their memory and bandwidth requirements.

Table 2: LCD displays

Name	X res	Y res	Refresh, Hz	BPP, bits	FrameSize, Mbytes	Bandwidth, MiB/s
TX09D50VM1CCA	240	320	60	24	0.22	13.18
TCG057VGLAC	640	480	60	24	0.88	52.73
GTTV57NN771E0	640	480	60	24	0.88	52.73
CLAA057VA01CW	640	480	60	24	0.88	52.73
RA158Z	800	480	60	24	1.1	65.92
GATW70SN8H1E0	800	600	60	24	1.37	82.4
CLAA080MB0ACW	800	600	60	24	1.37	82.4

2.6.6 High Speed MultiMedia Card Interface

The two High Speed Multimedia Card Interfaces (HSMCI) supports the MultiMedia Card (MMC) Specification V4.3, the SD Memory Card Specification V2.0, the SDIO V1.1 specification and CE-ATA V1.1. For CE-ATE external logic is required.

All CompactFlash modes (Attribute Memory, Common Memory, I/O and True IDE) are supported but the signals _IOIS16 (I/O and True IDE modes) and _ATA SEL (True IDE mode) are not handled.

2.6.7 Analog interface

Capture analog signals using 8-channel ADC. With and two Three-channel 16-bit Timer/Counters and the 4-channel PWM can be measured frequency and times, count pulses, generate delay timings, pulses and pulse width modulation.

2.6.8 Two-wire interface

The interface implements I^2C and SMBUS. This allows external temperature sensors, EEPROM to be used.

2.6.9 SPI controller

CAN controllers, ADCs and DACs, DataFlash and 3-wire EEPROM are attachable to module. The SPI capable devices can be connected as a Single Master/Multiple Slave or daisy chain.

2.6.10 AC97 controller

The AC97 Controller communicates with an audio codec (AC97) or a modem codec (MC'97) via the AC-link digital serial interface.

2.6.11 Image Sensor Interface

The Image Sensor Interface (ISI) connects a CMOS-type image sensor to the processor and provides image capture in various formats. It does data conversion, if necessary, before the storage in memory through DMA.

2.6.12 JTAG interface for debug and memory programming

Debugging and memory programming using PEEDI is easy.

3 SO-DIMM connector

The connector have to be SO-DIMM, 200 ways(pins), 2.5V, DDR type 1(DDR1), this is standard MO-224.

Recommended connector:
Molex: 78309-1130
FCI: 59354-052FSLF

Connectors SO-DIMM with 1.8V, DDR type 2(DDR2), standard MO-274 are NOT applicable!

3.1 Pinout diagram

v1.2 and v1.3 share the same pinout.
Table 3: M9G45-C Microprocessor v1.2 SO-DIMM 200 connector

M9G45-C Microprocessor			SODIMM200		M9G45-C Microprocessor		
Per. B	Per. A	I/O	B	A	I/O	Per. A	Per. B
		TX-	2	1	GND_BG		
		TX+	4	3	ETH_VDD		
		RX-	6	5	GND_S		
		RX+	8	7	PB7	RXD2	
		LED3	10	9	PB6	TXD2	
		LED2	12	11	LED1		
		D15	14	13	GND		
		D14	16	15	D7		
		D13	18	17	D6		
+3.3V			20	19	D5		
		D12	22	21	D4		
		D11	24	23	D3		
		D10	26	25	D2		
		D9	28	27	GND		
		D8	30	29	D1		
+3.3V			32	31	D0		
ISI_D10	TWD1	PB10	34	33	PC5	A22/NANDCLE	
ISI_D8	TXD3	PB8	36	35	PB9	RXD3	ISI_D9
	ISI_D6	PB26	38	37	PB27	ISI_D7	
GND			40	39	PB25	ISI_D5	
KEY							
	ISI_D4	PB24	42	41	GND		
	ISI_D2	PB22	44	43	PB23	ISI_D3	
Vcc_ISI			46	45	PB21	ISI_D1	
		A10	48	47	PB20	ISI_D0	
		A8	50	49	A9		
		A7	52	51	GND		
		A5	54	53	A6		
		A3	56	55	A4		
		A1	58	57	A2		
		+3.3V	60	59	A0		
PWM0	SPI0_nPCS1	PD24	62	61	PD6	AC97RX	
PCK1	ISI_MCK	PB31	64	63	PB0	SPI0_MISO	
	SPI0_SPCK	PB2	66	65	GND		
	A23	PC6	68	67	PD7	AC97TX	TIOA5
	SPI0_MOSI	PB1	70	69	PD0	TK0	PWM3
+3.3V			72	71	PD25	SPI0_nPCS2	PWM1
	TD1	PD10	74	73	PD19	SPI1_NPCS3	FIQ
	RD1	PD11	76	75	PB17	SPI1_nPCS0	RTS0
	RF1	PD15	78	77	PD12	TK1	PCK0
	NCS2	PC13	80	79	GND		
SDCS_nCS1			82	81	EBI1_WE/WR0/CFWE		
nRD/nOE/nCFOE			84	83	EBI1_BS1/WR1/CFIOR		
	ISI_VSYNC	PB29	86	85	EBI1_BS3/WR3/CFIOW		
+3.3V			88	87	PB30	ISI_HSYNC	
TCLK5	AC97CK	PD9	90	89	PD8	AC97FS	TIOB5
	A25_CFRNW	PC12	92	91	PC15	EBI1_nWAIT	
	CS5/CFCS1/CTS2	PC11	94	93	PC10	EBI1_nCS4/CFCS0	TCLK2
	CFCE1	PC8	96	95	GND		
	TXD1	PB4	98	97	PC9	CFCE2	RTS2
	RTS1	PD16	100	99	PB5	RXD1	
SPI0_nPCS2	TXD0	PB19	102	101	PD17	CTS1	
SPI1_nCS1	TSADTRIG	PD28	104	103	PB18	RXD0	SPI0_nPCS1

M9G45-C Microprocessor			SODIMM200		M9G45-C Microprocessor		
Per. B	Per. A	I/O	B	A	I/O	Per. A	Per. B
+3.3V			106	105	PD27	PCK1	SPI0_nPCS3
TCLK3	MCI0_CDA	PA1	108	107	PA2	MCI0_DA0	TIOB3
	SPI0_nPCS0	PB3	110	109	PA0	MCI0_CK	TCLK3
TIOA4	MCI0_DA2	PA4	112	111	PA3	MCI0_DA1	TCLK4
TIOB4	MCI0_DA3	PA5	114	113	GND		
	TWCK0	PA21	116	115	PA20	TWD0	
	DTXD	PB13	118	117	PB12	DRXD	
TSAD0*	TIOA0	PD20	120	119	PB28	ISI_PCK	
PWM2	PCK0	PD26	122	121	PD21	TIOA1	TSAD1*
+3.3V			124	123	PD18	IRQ	SPI1_nPCS2
TSAD2*	TIOA2	PD22	126	125	PD29	TCLK1	SCK1
RTS3	MCI1_DA0	PA23	128	127	PD23	TCLK0	TSAD3*
SCK2	TIOB0	PD30	130	129	PA24	MCI1_DA1	CTS3
PCK0	LCDPWR	PE0	132	131	GND		
	LCDMOD	PE1	134	133	PD14	TF1	
ISI_D11	TWCK1	PB11	136	135	PD1	TF0	
PWM3	MCI1_DA2	PA25	138	137	PD31	TIOB1	PWM1
	RK1	PD13	140	139	PA28	MCI1_DA5	ERXCK
+3.3V			142	141	PE31	PWM2	PCK1
	LCDHSYNC	PE4	144	143	PE3	LCDVSYNC	
	LCDEN	PE6	146	145	PE5	LCDDOTCK	
LCDD2	LCDD0	PE7	148	147	PE2	LCDCC	
LCDD4	LCDD2	PE9	150	149	PE8	LCDD1	LCDD3
LCDD5	LCDD3	PE10	152	151	GND		
LCDD7	LCDD5	PE12	154	153	PE11	LCDD4	LCDD6
LCDD11	LCDD7	PE14	156	155	PE13	LCDD6	LCDD10
LCDD12	LCDD8	PE15	158	157	PE16	LCDD9	LCDD12
+3.3V			160	159	PE17	LCDD10	LCDD14
LCDD18	LCDD12	PE19	162	161	PE18	LCDD11	LCDD15
LCDD20	LCDD14	PE21	164	163	PE20	LCDD13	LCDD19
LCDD22	LCDD16	PE23	166	165	PE22	LCDD15	LCDD21
	LCDD18	PE25	168	167	PE24	LCDD17	LCDD23
	LCDD19	PE26	170	169	GND		
	LCDD21	PE28	172	171	PE27	LCDD20	
	LCDD23	PE30	174	173	PE29	LCDD22	
	SPI1_MISO	PB14	176	175	PB16	SPI1_SPCK	SCK0
	SPI1_MOSI	PB15	178	177	WKUP		
+3.3V			180	179	SHDN		
MCI0_DA6	ERX2	PA8	182	181	PWR_EN		
MCI0_DA7	ERX3	PA9	184	183	VBAT		
GND			186	185	GND		
		HDDA+	188	187	nRST		
		HDDA-	190	189	RTCK		
+3.3V			192	191	TDO		
		DD+	194	193	nTRST		
		DD-	196	195	TDI		
GND			198	197	TCK		
NC			200	199	TMS		

3.2 Signal description

v1.2 and v1.3 share the same signals.

Table 4: M9G45-C Microprocessor v1.2 signals

I/O Line	Peripheral A	Peripheral B	CPU Module	SODIMM200	NOTE
PA0	MCI0_CK	TCLK3		PIN_109	
PA1	MCI0_CDA	TIOA3		PIN_108	
PA2	MCI0_DA0	TIOB3		PIN_107	
PA3	MCI0_DA1	TCLK4		PIN_111	
PA4	MCI0_DA2	TIOA4		PIN_112	
PA5	MCI0_DA3	TIOB4		PIN_114	
PA6	MCI0_DA4	ETX2	version codding		

I/O Line	Peripheral A	Peripheral B	CPU Module	SODIMM200	NOTE
PA7	MCI0_DA5	ETX3	version codding		
PA8	MCI0_DA6	ERX2		PIN_182	
PA9	MCI0_DA7	ERX3		PIN_184	
PA10	ETX0		PHY		
PA11	ETX1		PHY		
PA12	ERX0		PHY		
PA13	ERX1		PHY		
PA14	ETXEN		PHY		
PA15	ERXDV		PHY		
PA16	ERXER		PHY		
PA17	ETXCK		PHY		
PA18	EMDC		PHY		
PA19	EMDIO		PHY		
PA20	TWD0			PIN_115	
PA21	TWCK0			PIN_116	
PA22	MCI1_CDA	SCK3	NAND_CS1		
PA23	MCI1_DA0	RTS3		PIN_128	
PA24	MCI1_DA1	CTS3		PIN_129	
PA25	MCI1_DA2	PWM3		PIN_138	
PA26	MCI1_DA3	TIOB2			
PA27	MCI1_DA4	ETXER	NAND_CS2		
PA28	MCI1_DA5	ERXCK		PIN_139	
PA29	MCI1_DA6	ECRS	NAND_CS3		
PA30	MCI1_DA7	ECOL			
PA31	MCI1_CK	PCK0	1-wire (DS2401)		

Table 5: M9G45-C Microprocessor v1.2 signals

I/O Line	Peripheral A	Peripheral B	CPU Module	SODIMM200	NOTE
PB0	SPI0_MISO		DataFlash	PIN_063	
PB1	SPI0_MOSI		DataFlash	PIN_070	
PB2	SPI0_SPCK		DataFlash	PIN_066	
PB3	SPI0_NPCS0		DataFlash	PIN_110	100k pullup
PB4	TXD1			PIN_098	
PB5	RXD1			PIN_099	
PB6	TXD2			PIN_009	
PB7	RXD2			PIN_007	
PB8	TXD3	ISI_D8		PIN_036	
PB9	RXD3	ISI_D9		PIN_035	
PB10	TWD1	ISI_D10		PIN_034	
PB11	TWCK1	ISI_D11		PIN_136	
PB12	DRXD			PIN_117	
PB13	DTXD			PIN_118	
PB14	SPI1_MISO			PIN_176	
PB15	SPI1_MOSI	CTS0		PIN_178	
PB16	SPI1_SPCK	SCK0		PIN_175	
PB17	SPI1_NPCS0	RTS0		PIN_075	
PB18	RXD0	SPI0_NPCS1		PIN_103	
PB19	TXD0	SPI0_NPCS2		PIN_102	
PB20	ISI_D0			PIN_047	
PB21	ISI_D1			PIN_045	
PB22	ISI_D2			PIN_044	
PB23	ISI_D3			PIN_043	
PB24	ISI_D4			PIN_042	
PB25	ISI_D5			PIN_039	
PB26	ISI_D6			PIN_038	
PB27	ISI_D7			PIN_037	
PB28	ISI_PCK			PIN_119	
PB29	ISI_VSYNC			PIN_086	
PB30	ISI_HSYNC			PIN_087	
PB31	ISI_MCK	PCK1		PIN_064	

Table 6: M9G45-C Microprocessor v1.2 signals

I/O Line	Peripheral A	Peripheral B	CPU Module	SODIMM200	NOTE
PC0	DQM2				
PC1	DQM3				
PC2	A19				

I/O Line	Peripheral A	Peripheral B	CPU Module	SODIMM200	NOTE
PC3	A20				
PC4	A21/NANDALE		NAND_ALE		
PC5	A22/NANDCLE		NAND_CLE	PIN_033	22R serial
PC6	A23			PIN_068	22R serial
PC7	A24				
PC8	CFCE1			PIN_096	22R serial
PC9	CFCE2	RTS2		PIN_097	22R serial
PC10	NCS4/CFCS0	TCLK2		PIN_093	22R serial
PC11	NCS5/CFCS1	CTS2		PIN_094	22R serial
PC12	A25/CFRNW			PIN_092	22R serial
PC13	NCS2			PIN_080	22R serial
PC14	NCS3/NANDCS		NAND_CS0		
PC15	NWAIT			PIN_091	22R serial
PC16	D16				
PC17	D17				
PC18	D18				
PC19	D19				
PC20	D20				
PC21	D21				
PC22	D22				
PC23	D23				
PC24	D24				
PC25	D25				
PC26	D26				
PC27	D27				
PC28	D28				
PC29	D29				
PC30	D30				
PC31	D31				

Table 7: M9G45-C Microprocessor v1.2 signals

I/O Line	Peripheral A	Peripheral B	CPU Module	SODIMM200	NOTE
PD0	TK0	PWM3		PIN_069	
PD1	TF0			PIN_135	
PD2	TD0		enable/disable 50MHz osc. (1/0)		
PD3	RD0		NAND RD/BY		
PD4	RK0				
PD5	RF0		PHY		
PD6	AC97RX			PIN_061	
PD7	AC97TX	TIOA5		PIN_067	
PD8	AC97FS	TIOB5		PIN_089	
PD9	AC97CK	TCLK5		PIN_090	
PD10	TD1			PIN_074	
PD11	RD1			PIN_076	
PD12	TK1	PCK0		PIN_077	22R serial
PD13	RK1			PIN_140	
PD14	TF1			PIN_133	
PD15	RF1			PIN_078	
PD16	RTS1			PIN_100	
PD17	CTS1			PIN_101	
PD18	SPI1_NPCS2	IRQ		PIN_123	
PD19	SPI1_NPCS3	FIQ		PIN_073	
PD20	TIOA0			PIN_120	
PD21	TIOA1			PIN_121	
PD22	TIOA2			PIN_126	
PD23	TCLK0			PIN_127	
PD24	SPI0_NPCS1	PWM0		PIN_062	
PD25	SPI0_NPCS2	PWM1		PIN_071	
PD26	PCK0	PWM2		PIN_122	
PD27	PCK1	SPI0_NPCS3		PIN_105	
PD28	TSADTRG	SPI1_NPCS1		PIN_104	
PD29	TCLK1	SCK1		PIN_125	
PD30	TIOB0	SCK2		PIN_130	
PD31	TIOB1	PWM1		PIN_137	

Table 8: M9G45-C Microprocessor v1.2 signals

I/O Line	Peripheral A	Peripheral B	CPU Module	SODIMM200	NOTE
PE0	LCDPWR	PCK0		PIN_132	
PE1	LCDMOD			PIN_134	
PE2	LCDCC			PIN_147	
PE3	LCDVSYNC			PIN_143	22R serial
PE4	LCDHSYNC			PIN_144	22R serial
PE5	LCDDOTCK			PIN_145	22R serial
PE6	LCDDEN			PIN_146	22R serial
PE7	LCDD0	LCDD2		PIN_148	22R serial
PE8	LCDD1	LCDD3		PIN_149	22R serial
PE9	LCDD2	LCDD4		PIN_150	22R serial
PE10	LCDD3	LCDD5		PIN_152	22R serial
PE11	LCDD4	LCDD6		PIN_153	22R serial
PE12	LCDD5	LCDD7		PIN_154	22R serial
PE13	LCDD6	LCDD10		PIN_155	22R serial
PE14	LCDD7	LCDD11		PIN_156	22R serial
PE15	LCDD8	LCDD12		PIN_158	22R serial
PE16	LCDD9	LCDD13		PIN_157	22R serial
PE17	LCDD10	LCDD14		PIN_159	22R serial
PE18	LCDD11	LCDD15		PIN_161	22R serial
PE19	LCDD12	LCDD18		PIN_162	22R serial
PE20	LCDD13	LCDD19		PIN_163	22R serial
PE21	LCDD14	LCDD20		PIN_164	22R serial
PE22	LCDD15	LCDD21		PIN_165	22R serial
PE23	LCDD16	LCDD22		PIN_166	22R serial
PE24	LCDD17	LCDD23		PIN_167	22R serial
PE25	LCDD18			PIN_168	22R serial
PE26	LCDD19			PIN_170	22R serial
PE27	LCDD20			PIN_171	22R serial
PE28	LCDD21			PIN_172	22R serial
PE29	LCDD22			PIN_173	22R serial
PE30	LCDD23			PIN_174	22R serial
PE31	PWM2	PCK1		PIN_141	
			WKUP	PIN_177	Wakeup
			SHDN	PIN_179	Shutdown/Standby
			PWR_EN	PIN_181	Enabel regulators

3.2.1 Ethernet signals

Signal TX-, TX+ RX- and RX+ are for connecting of the Ethernet transceiver(PHY) to the Ethernet magnetic module(trafo). LED1, LED2 and LED3 are the PHY's LED_LINK, LED_ACT and LED_SPEED through 100Ohm resistance. GND_BG and 3V_ETH are the analog receive/transmit power supply, which is usually connected to the transformer or combined RJ45 connector.

Analog receive/transmit power voltage depend on the PHY chip, see Table 1 PHY chips .

3.2.2 External Bus Interface signals

D0-D15 formates the EBI data bus and A0-A10, A23, A24 and A25 formates the EBI address bus.

3.2.3 USB signals

To use the USB Port B as an USB OTG, choose one free pin to act as PIO input, and software should monitor this pin to select host or device behaviour.

3.2.4 Power control signals

The WKUP signal turn the MCU to active state, and has a 100Kohm pull-up to VBAT. The SHDN signal brings the MCU to power down state. The PWR_EN signal enables the MCU internal circuits power supply, it must be connected to GND to enable on-board regulators. The VBAT maximum power voltage is 4V(check AT91SAM9G45 electrical characteristics).

The ADC power lines a wired to the main 3.3V VDD and the common GND.

3.2.5 PIO signals for BB9263

PD18 is used as a touch screen interrupt sygnal. PE31 is a a touch screen busy pin. PD14 is used to reset the CompactFlash. PD1 is assigned for USB detection. PD31 is a LED2. PB6 and PB7 are for ISI_VCTRL1 and ISI_VCTRL2.

3.2.6 Interrupt Request(FIQ/IRQ)

A FIQ and IRQ pins is available for managing external events.

3.2.7 Image sensor interface

The VCC_ISI pins is the power supply for PIO port B and it should be wired to +3.3V power line.

3.2.8 JTAG and TAP controller

The TRST signal has a 1K pull-down which ensures proper booting of the CPU.

4 Technical specifications

4.1 Temperature

M9G45-C Microprocessor is available in two temperature ranges:

- Standard temperature range 0℃ +70℃
- Industrial temperature range -40℃ +85℃

4.2 Electrostatic Warning

The M9G45-C Microprocessor Module is shipped in protective anti-static packaging. The board must not be subjected to high electrostatic potentials. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the component pins or any other metallic element.

4.3 RoHS Compliance Statement

The product is fully RoHS Compliant.

A RoHS signed declaration for use of RoHS processes and materials is available.

4.4 Compatibility with PM9263

For M9G45-C Microprocessor v1.2, v1.3 and BB9263 v1.1:

- on BB9263 remove resistor R66 - fixes USB device port
  The software for AT91SAM9G45-EK(RomCode and so on) uses internal pullup for USB Device Port (Data+ signal). The BB9263 is not made for GPIO controlled Data+ pullup.
- on BB9263 remove capacitors C40 and C41 - fixes USB host High Speed
- on BB9263 remove capacitor C81 - fixes USB device High Speed

Compatible with the base board for PM9263(BB9263).

4.5 Module versions

v1.3	beginning 2011, in production	- added SPI Flash - DP83848 replaced by DM9161A/B - 2.2uF 1206 replaced by 100nF 0402 - added 12MHz oscillator

v1.2	beginning 2010, in production	- removed second 1.8V regulator - removed DDR2 connected to EBI1 - removed level shifters and their pull-ups - added two mounting holes 2.2mm - placed on the top left and right corner - added PA8, PA9, PA28 to 200-pin connector
v1.1	2010, discontinued	- corrected power supply of all DDR2 chips - inverted signal EN_1V2 - removed R34 - overlap R1 and R4 to eliminate the possibility to assemble both - changed from 220R to 1K: R58, R72, R73, R74, R78, R79, R80, R82, R83, R84, R85

4.6 Not populated elements

Some elements are not populated, and some are alternative. Take a look at table Table 9 Not populated elements . To request a specific population get in contact with Ronetix.

Table 9: Not populated elements

Element	Description
Y4, C82	instead of Y2
R100	Ready/Busy depending on NAND chip pinout
R107	NAND CSs depending on NAND chip pinout
U2 or U6 or U17	populate either U2 or U17 or U6. DataFlash is an optional component.
R8, R9	board version ID
R37	selects led function of the PHY
R28, R29, R36 and Q2	ETH0_LED1 driver, fix PHY DM9161B led bug

4.7 Order and information

For order and information requests please write an e-mail to sales@ronetix.at or info@ronetix.at.