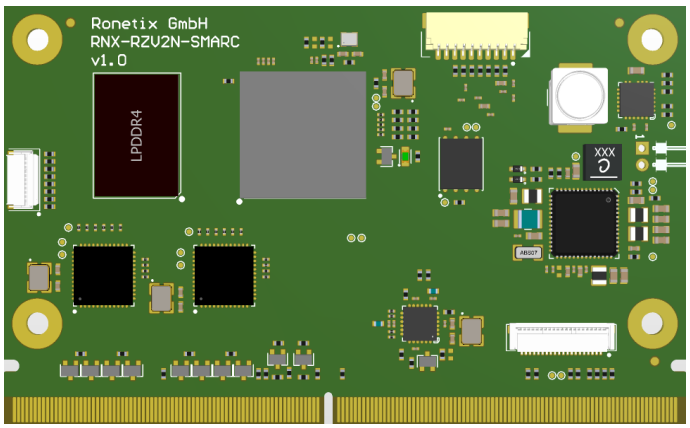
High-performance System on Module (SOM)

RNX-RZV2N-SMARC

SMARC Module with Renesas RZ/V2N

Datasheet

rev 1.0



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1. Document Revision History

Revision	Date	Notes
1.0	06.03.2025	Initial release

2. Table of Contents

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3. Overview

3.1 General Information

The **RNX-RZV2N-SMARC** is a high-performance CPU Module (SoM – System On Module) designed for a range of AI-driven vision applications. It is based on the Renesas RZ/V2N CPU and includes 1.8 GHz Quad Arm® Cortex®-A55 on-chip FPU, Neon™, L1-caches and L3-cache, 200MHz Arm® Cortex®-M33 on-chip FPU and DSP-extension, DRP-AI, Mali™-G31 (GE3D), Mali™-C55 (ISP), 1.5 MB of on-chip SRAM, 2ch GbEthernet MAC, 1ch USB2.0, USB3.2 Gen 2x1, 2-MIPI® CSI-2® camera input interface, 1-MIPI® DSI® video output interface, PCIe® Gen3 2Lane (EP/RC), various communication interfaces such as xSPI, eMMC™, I2S (TDM), I3C®, PDM, and security functions.

3.2 Highlights

CPU	• 4x Armv8.2-A, 64-bit Cortex™-A55 Core, 1.8 GHz • ARM® Cortex™-M33, 200 MHz • AI accelerator DRP-AI (AI-MAC+DRP) • 15 sparse TOPS, 4 dense TOPS • 3D Graphics Engine: Arm Mali-G31 • Image Signal Processor: Arm Mali-C55 • H.264/H.265 codec module • Image Scaling Unit
Memory	• RAM: 4 GiB LPDDR4X, 32-bit bus (up to 8 GiB) • eMMC: 16 GiB (optional: up to 256 GiB) • SPI NOR Flash (optional 128 MBit)
Display	• MIPI DSI, up to 1920x1200, 60Hz
Camera	• Up to 2x MIPI-CSI, 4 data lanes
Network	• Ethernet: 2x 1 Gbps ports
I/O	• 1x PCI Express x2 Gen. 3 • Up to 4x USB 2.0 host ports • 1x USB 3.2 Host • Up to 1x USB 2.0 OTG port • 4x UART ports • MMC/SD/SDIO • 2x SPI • 5x I2C • 12x GPIOs
Electrical	• Supply Voltage: 5.0V
Physical	• Board size: SMARC (Smart Mobility ARChitecture), 82x50mm • Operation temperature: 0° +70°C, -20° to 85° C (optional) • Relative humidity: 10% to 90%

3.3 SoM Block Diagram

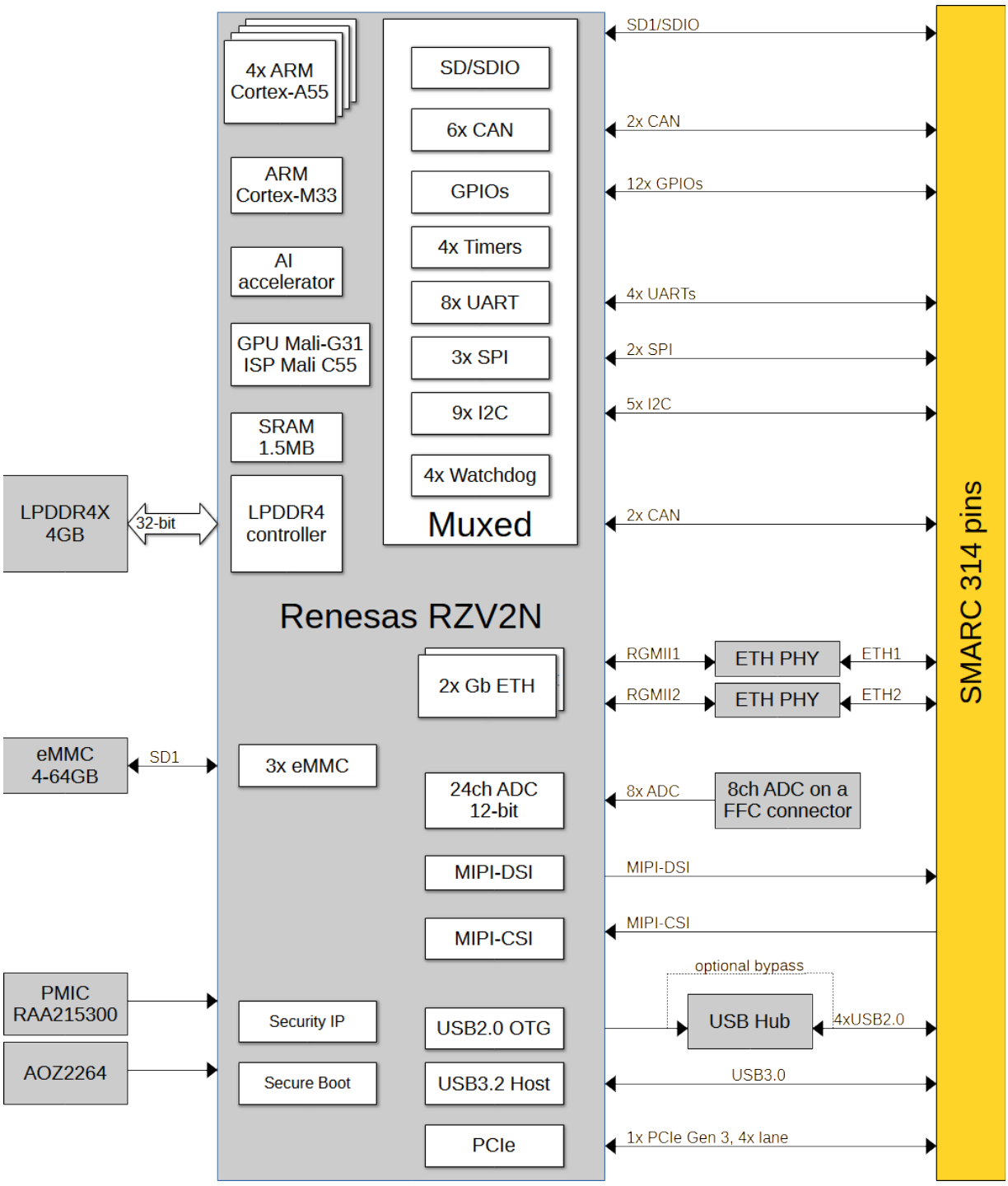

Figure 3.1: SoM block diagram

4. CPU Module Hardware Components

This chapter describes the hardware components of RNX-RZV2N-SMARC SoM.

4.1 Power supply

RNX-RZV2N-SMARC uses Renesas's RAA215300 as a Power Management Integrated circuit (PMIC) designed specifically for use with Renesas's processors. The PMIC and the additional AOZ2264NQI-11 synchronous buck regulator provide all power rails required on CPU module from a single 5.0V power supply.

The PMIC is fully programmable via the I2C interface and associated register map. Additional communication is provided by direct logic interfacing including interrupt, watchdog and reset.

4.2 CPU RZ/V2N

The RZ/V2N AI MPU boasts Renesas' proprietary dynamically reconfigurable processor AI accelerator (DRP-AI), quad Arm® Cortex®-A55 (1.8GHz) Linux processors, and Cortex®-M33 (200MHz) real-time processors. Furthermore, the RZ/V2N also includes another dynamically reconfigurable processor (DRP). This processor can accelerate image processing, such as OpenCV, and dynamics calculations required for robotics applications. It also features high-speed interfaces like PCIe®, USB 3.2, and Gigabit Ethernet, making it an ideal microprocessor for applications such as autonomous robots and machine vision in factory automation, where advanced AI processing must be implemented with low power consumption. The RZ/V2N part is particularly useful for applications such as:

- High-Performance Vision AI System
- Smart Robot Vacuum Cleaner
- Industrial — Gateway, Scanner, Printer, Ruggedized HMI, Factory Automation, Robotic Controller, Machine Visual Inspection, Digital Kiosk, Digital Signage, Vision Payment Systems, Industrial PCs
- Medical — Pumps/Respirator/Clinical Monitoring

4.2.1 CPU Block Diagram

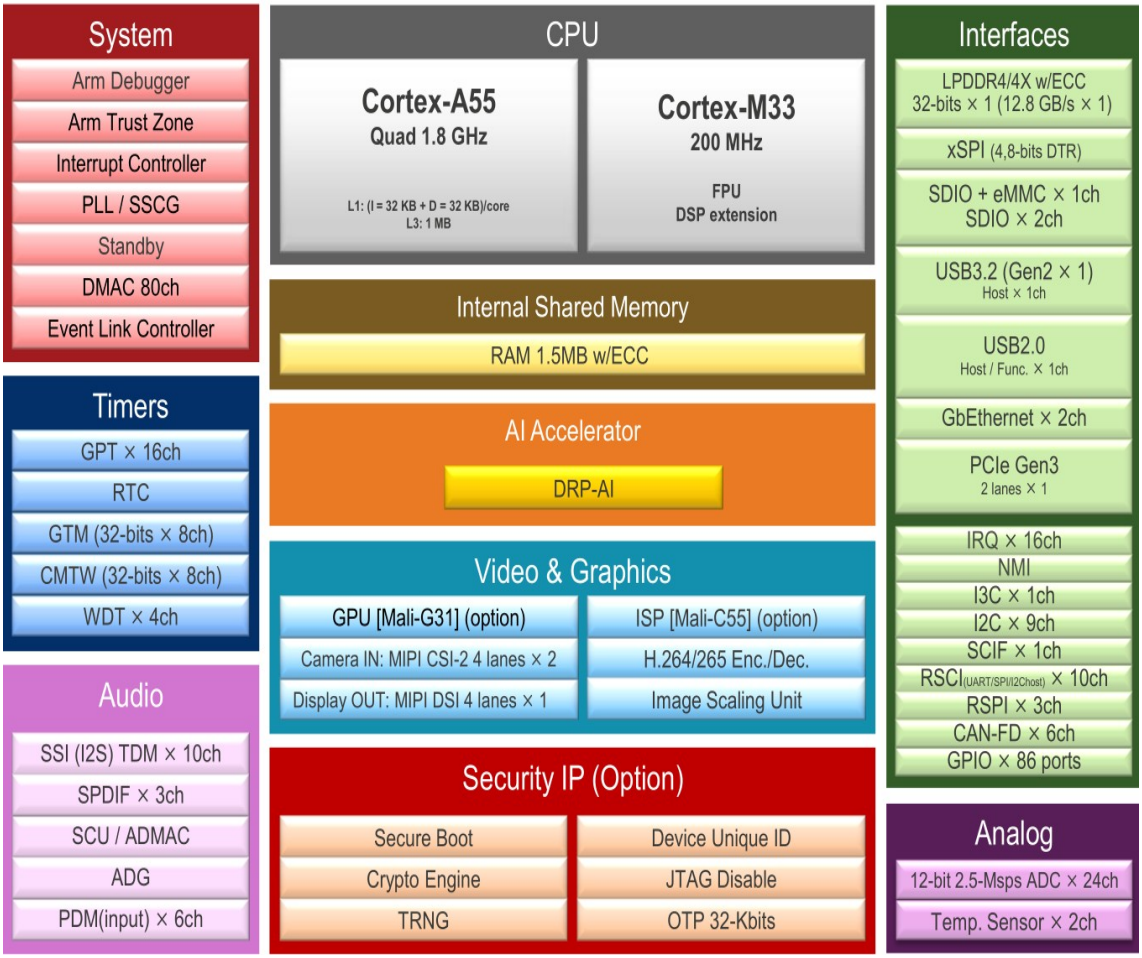

Figure 4.1: RZ/V2N block diagram

4.2.2 CPU Platform

The RZ/V2N processor implements 4x ARM® Cortex®-A55 cores intended for high level O/S and an ARM® Cortex®-M33 core dedicated for real-time and security tasks.

The ARM Cortex-A55 platform has the following features:

- 4x ARM Cortex-A55 Cores
- Target frequency of 1.8GHz
- The core configuration is symmetric, where each core includes:

  - L1 cache: I-Cache 32 Kbyte, D-Cache 32Kbytes
  - L2 cache: 0 Kbyte
  - L3 cache: 1 Mbyzeswith ECC
  - MMU supported
  - Neon™ and FPU supported
  - Cryptographic extension supported
  - Armv8-A architecture
- AI accelerator
  - DRP-AI (AI-MAC + DRP)
  - Up to 4 dense TOPS
  - Up to 15 sparse TOPS

The ARM Cortex-M33 platform includes the following features:

- 1× Cortex-M33 processor
- FPU supported
- DSP extension supported
- Security extension supported
- Armv8-M architecture

4.3 Memory

4.3.1 DRAM

RNX-RZV2N-SMARC is standard equipped with 4 GB LPDDR4X memory. Optionally up to 8 GB 3.2GT/s can be assembled. The data bus is 32-bit wide.

4.3.2 eMMC

RNX-RZV2N-SMARC is standard equipped with 16 GB eMMC. Optionally up to 256 GB can be assembled.

The eMMC can be used as boot device.

4.3.3 SPI NOR Flash

RNX-RZV2N-SMARC is optionally equipped with 128 MBit SPI NOR Flash. The SPI NOR Flash is connected to the RZ/V2N SoC xSPI interface. The QSPI can be used as boot device.

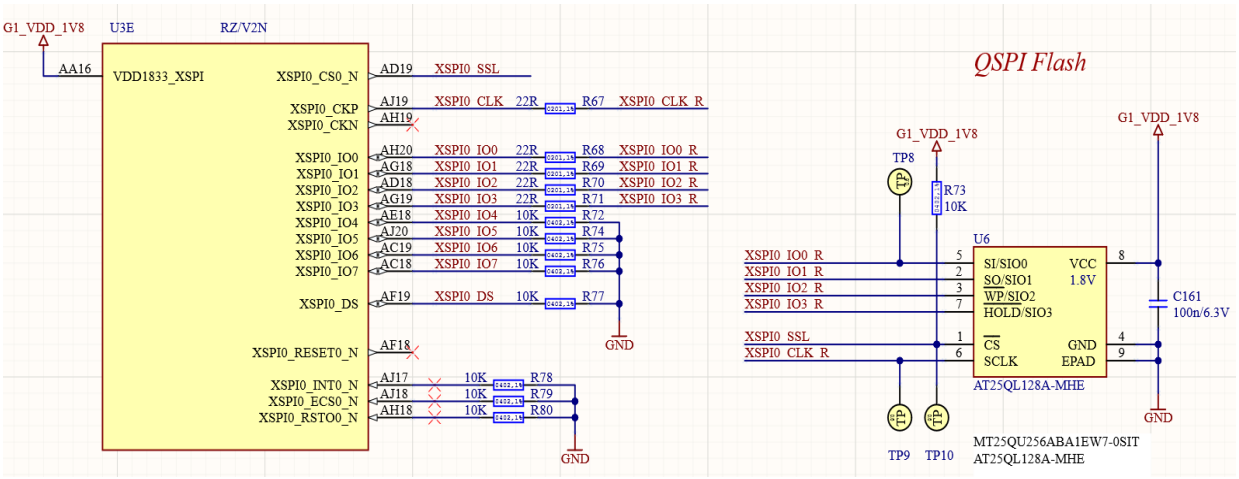

Figure 4.2: Octal-SPI NOR Flash

4.4 USB Hub

An optional USB Hub USB2534, connected to USB2, can be populated. In this case four additional USB ports (USBHUB1, USBHUB2, USBHUB3, USBHUB4) are available on the SMARC connector.

5. SMARC 314-pin connector

The RNX-RZV2N-SMARC exposes a 314-pin MXM 3 connector.

6. CPU Module interfaces

6.1 Gigabit Ethernet

RNX-RZV2N-SMARC implements two full-featured 10/100/1000 Ethernet ports implemented with MACs built into the RZ/V2N SoC, coupled with KSZ9131RN RGMII Ethernet PHYs from Microchip.

Both interfaces support the following main features:

- 10/100/1000 BASE-T IEEE 802.3 compliant.
- Compliant with IEEE802.1Qav, IEEE802.1Qat, and IEEE802.1AS.
- Compliant with IEEE1588-2008 with nano second timer in ch. 0 (main) and ch. 1 (sub).
- Support for full duplex and half duplex.
- Automatic MDI/MDIX crossover.
- Automatic polarity correction.
- Activity and speed indicator LED controls.

6.1.1 PCIe

The RZ/V2N SoC is equipped with one PCIe interfaces x4 Gen 3 which is provided on the SMARC connector. The 100MHz PCIe reference clock is generated on the SoM.

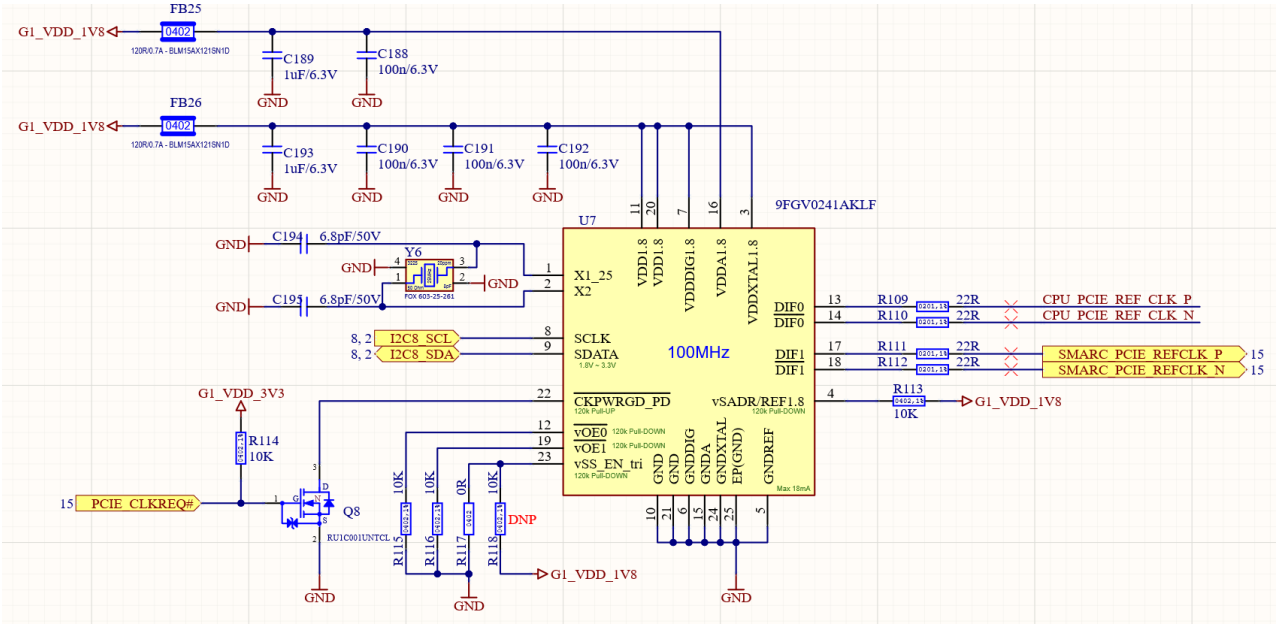

Figure 6.1: PCIe clock generator

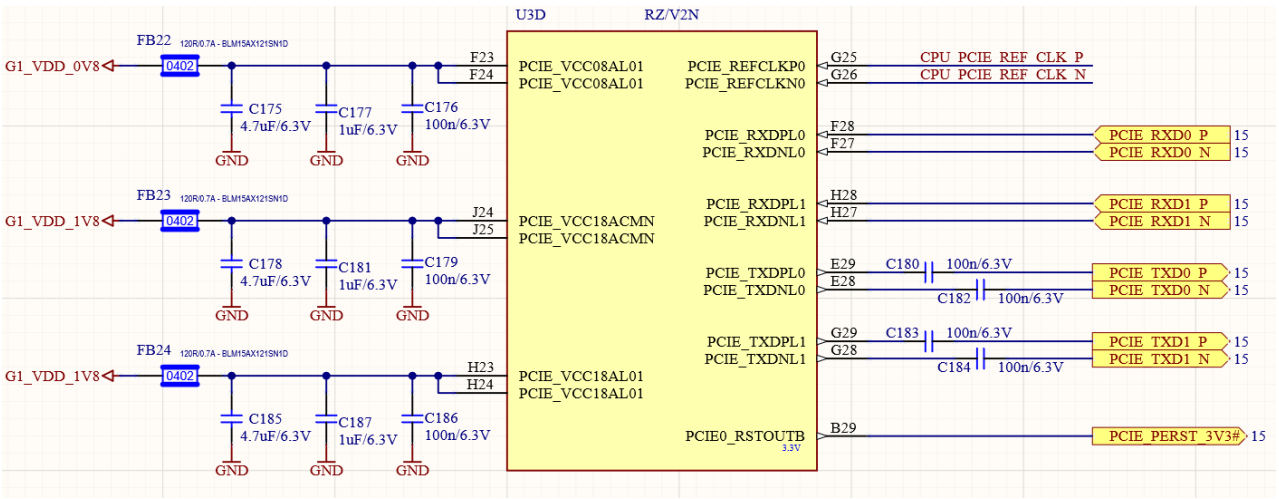

Figure 6.2: PCIe CPU side

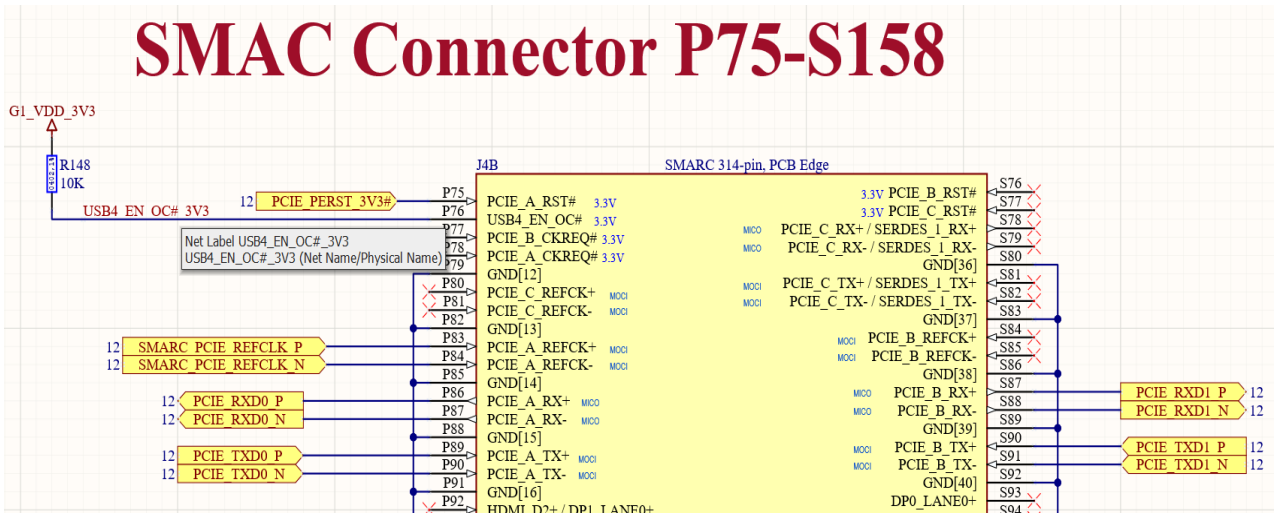

Figure 6.3: PCIe on SMARC connector

6.2 Display interface

RZ/V2N SoC MIPI-DSI signals are provided on SMARC connector, S125-S141

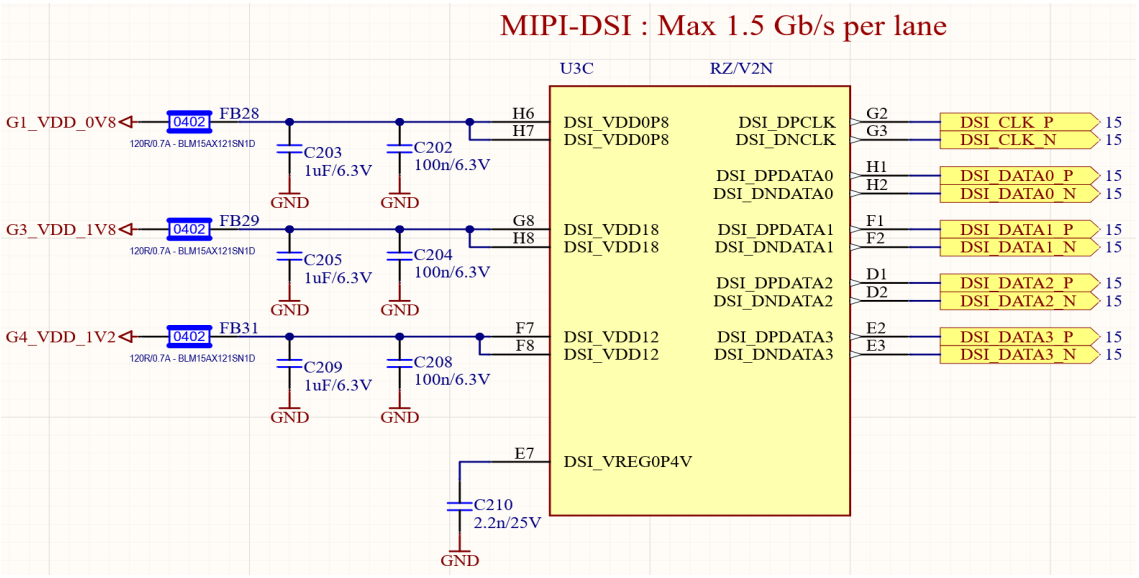

Figure 6.4: MIPI-DSI – CPU side

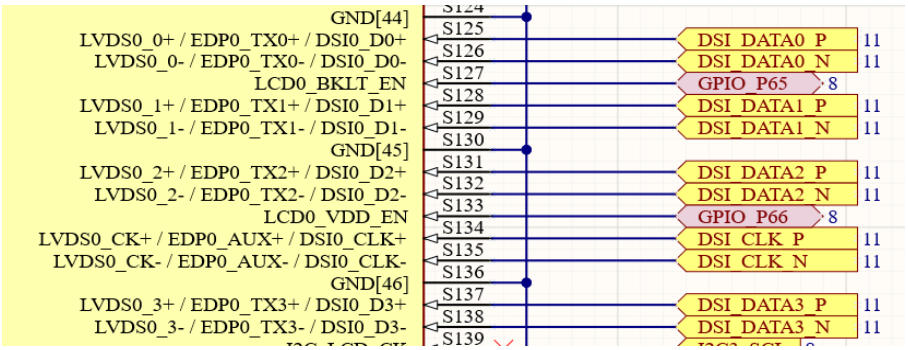

Figure 6.5: MIPI-DSI – SMARC connector

- MIPI DSI

  The DSI controller provides an interface that allows communication between the processor and MIPI DSI-compliant display devices. The MIPI-DSI interface is based on the four-lane MIPI display interface available with the RZ/V2N SoC.

  The key features of the MIPI DSI (controller and PHY) include:

  - Conforms to MIPI-DSI specification v1.2 and MIPI-DPHY specification v1.2

- Up to 1.5 Gbps per lane
- Up to four data lanes
- Support for the throughput up to 1920 × 1200 RGB888 60 fps
- Support for the throughput up to 1280 × 1024 RGB888 120 fps
- Support for 2-plane blending
- Support for image processing:
  - ✔ Dither processing (RGB666)
  - ✔ Clipping
  - ✔ RGB gamma correction LUT
- Support for input data formats:
  - ✔ RGB565, RGB666, RGB888
  - ✔ ARGB1555, ARGB4444, ARGB8888
  - ✔ YUV (YcbCr) 444 8-bits, YUV (YcbCr) 422 8-bits, YUV (YcbCr) 420 8-bits
- Support for output data formats:
  - ✔ RGB666, RGB888

6.3 MIPI-CSI Camera interface

The MIPI-CSI interface is based on the dual channel four-lane MIPI camera interface available with the RZ/V2N SoC. On RNX-RZV2N-SMARC MIPI-CSI0 is available on the SMARC connector as CSI0 with 2-lanes, the MIPI-CSI1 signals are available on the SMARC connector as CSI1 with 4-lanes.

The MIPI D-PHY includes the following features:

- Complies with MIPI standard CSI2 Version 2.1
- Supports both high speed, low power and Ultra-Low Power State modes
- Each lane runs at 2.1 Gbps
- Support for the throughput up to 4K RAW12 30 fps
- Support for 4 virtual channels selected from VC0 to VC15

- Support for input data formats:
  - YUV422 8 bits or 10 bits
  - RGB444, RGB555, RGB565, RGB666, RGB888
  - RAW6, RAW7, RAW8, RAW10, RAW12, RAW14, RAW16, RAW20
  - YUV420 8-bits or 10-bits (image processing not supported)
  - Legacy YUV420 8-bits (image processing not supported)
  - YUV420 8-bits or 10-bits (chroma shifted pixel sampling) (image processing not supported)
  - User defined byte-based data

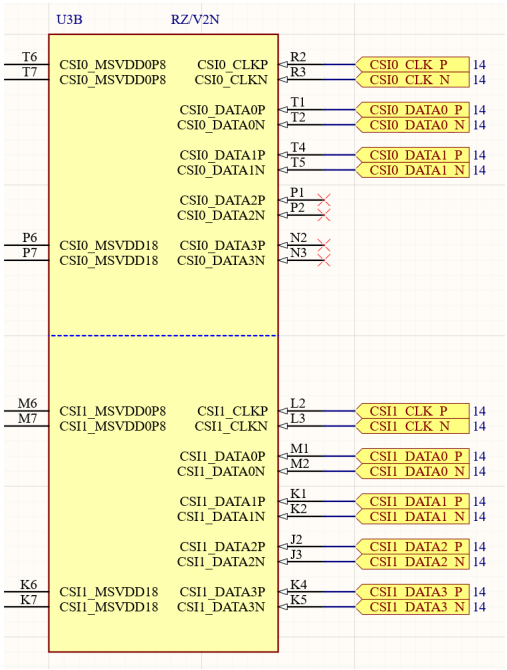

Figure 6.6: MIPI-CSI on CPU

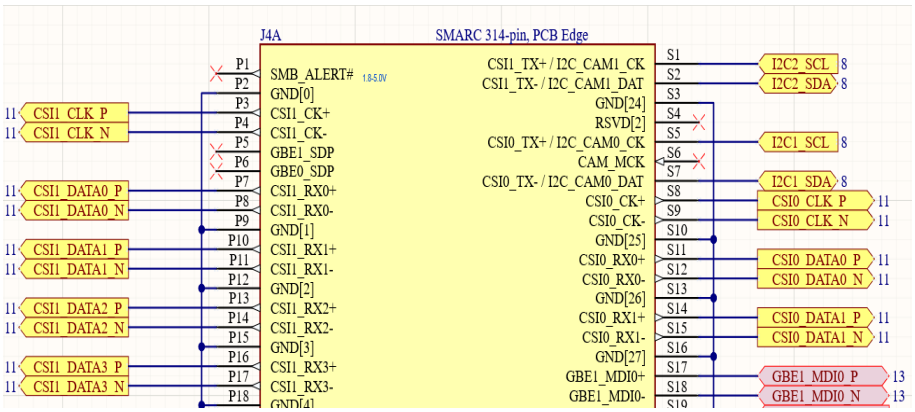

Figure 6.7: MIPI-CSI on SMARC connector

6.4 USB interface

The RZ/V2N SoC is equipped with two USB controllers and PHYs. One USB instance contains a USB 3.2 core, the second contains a USB 2.0 core. The USB 2.0 port supports dual-role functionality, the USB 3.2 port supports only host-role.

On RNX-RZV2N-SMARC USB 3.2 is available on the SMARC connector as USB2 port. USB 2.0 can be connected to the SMARC USB0 or connected to a 4-port USB Hub (assembly option). In the second case, USBHUB1, USBHUB2, USBHUB3 and USBHUB4 are connected to the SMARC connector.

6.4.1 USB 3.2

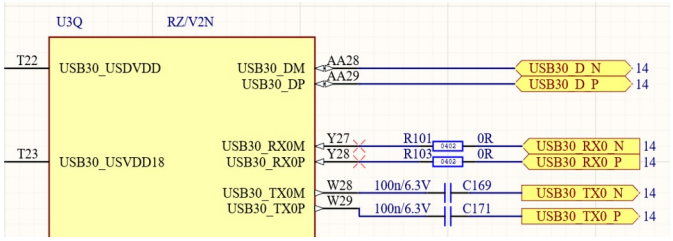

Figure 6.8: USB 3.2 CPU side

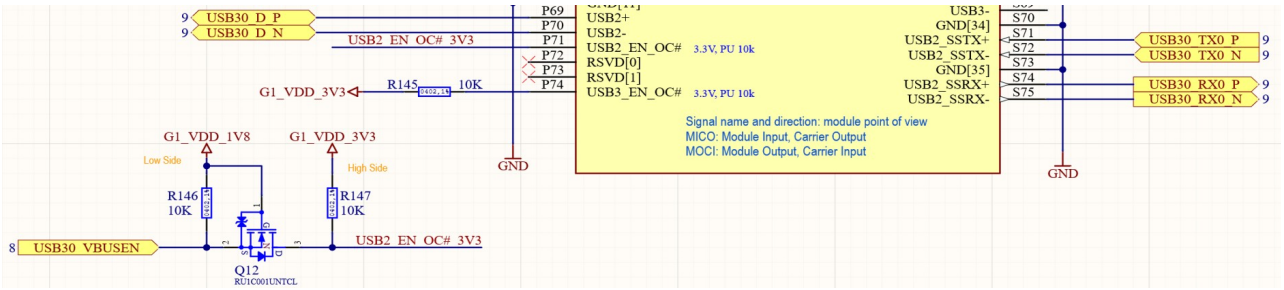

Figure 6.9: USB 3.2 SMARC connector

6.4.2 USB 2.0

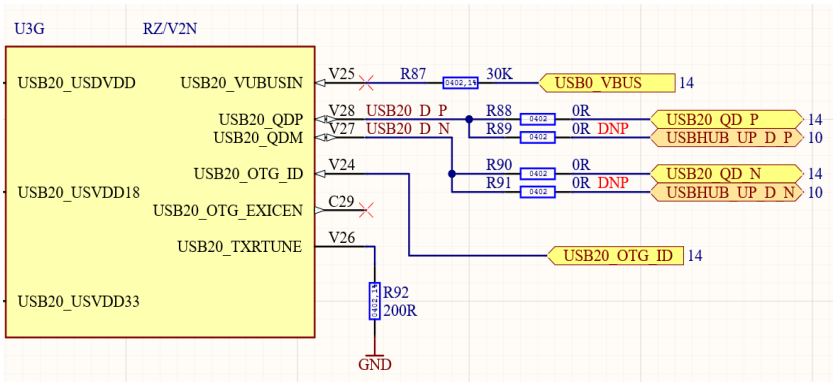

Figure 6.10: USB 2.0 CPU side

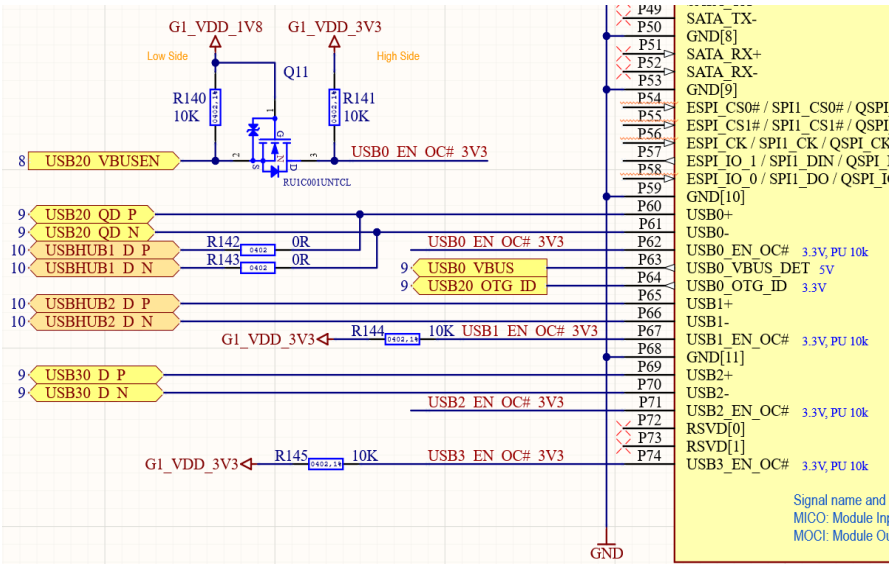

Figure 6.11: USB 2.0 SMARC connector

6.4.3 4-port USB Hub

When the USB Hub is assembled, the ports are connected to the SMARC connector as follows:

- USB Hub Port 1 – SMARC USB0 (P60, P61)
- USB Hub Port 1 – SMARC USB1 (P65, P66)
- USB Hub Port 3 – SMARC USB3 (S68, S69)
- USB Hub Port 4 – SMARC USB4 (S35, S36)

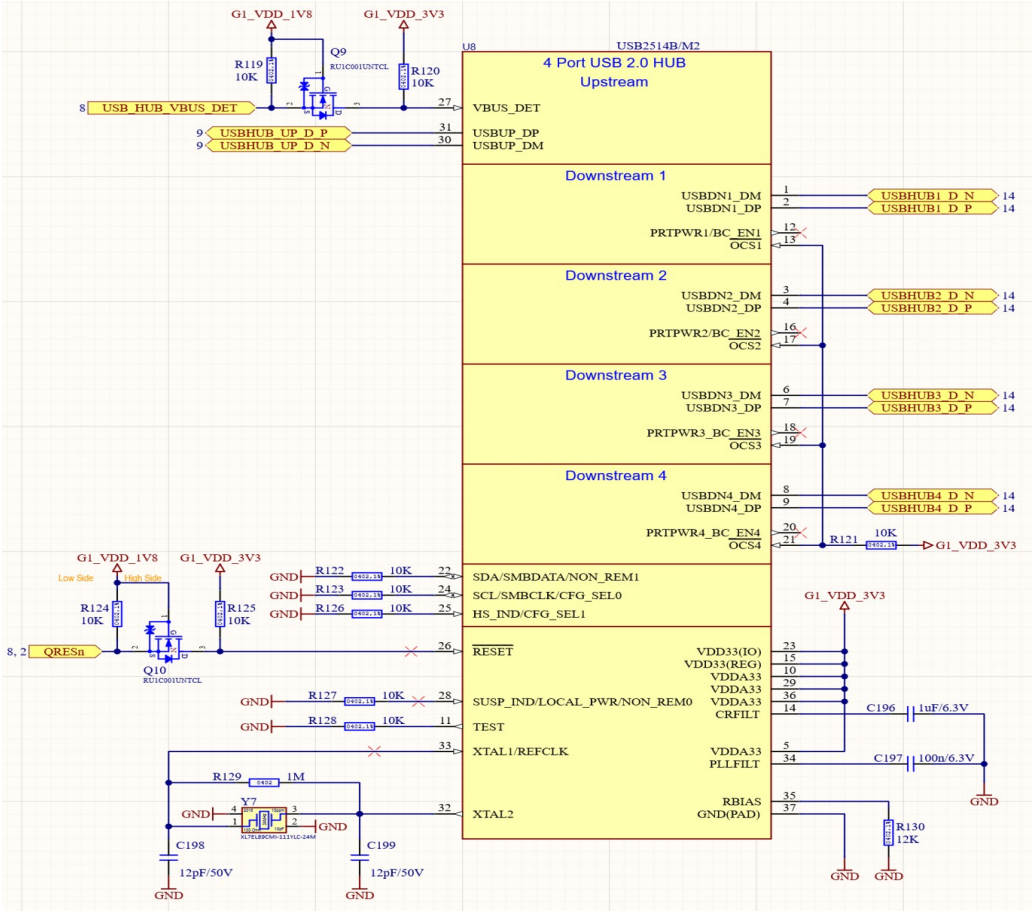

Figure 6.12: 4-port USB Hub

6.5 MMC, SD, SDIO

The RZ/V2N SoC is equipped with 3x MMC/SD/SDIO controller IPs. On RNX-RZV2N-SMARC SD0 is connected to the eMMC, SD1 is available on the SMARC connector.

The SD/MMC host interface supports the following main features:

- Channel 0 supports SDHI/e-MMC, 1/4/8-bit
- Channel 1 supports SDHI, 1/4-bit
- Default, high-speed, UHS-I/SDR50, and SDR104 and DDR50transfer modes
- Error check function: CRC7 (for command/response), CRC16 (for data)
- Backward-compatible, high-speed, HS-DDR and HS200 transfer modes supported

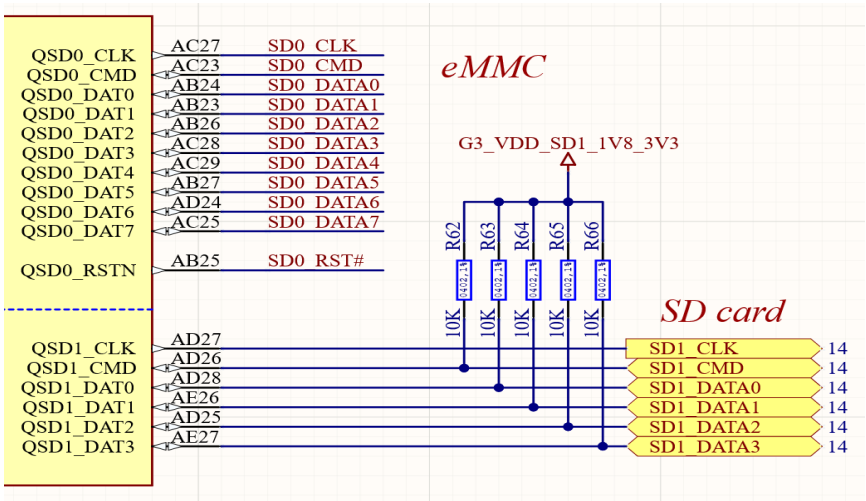

Figure 6.13: SD0, SD1 CPU side

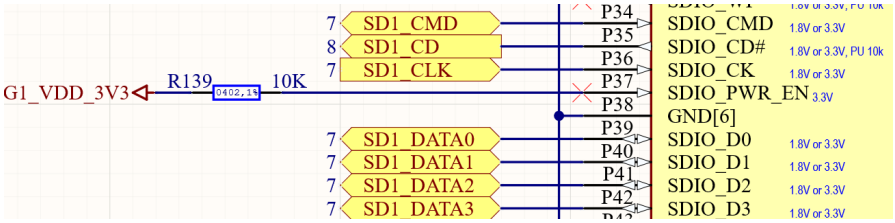

Figure 6.14: SD1 SMARC connector

6.6 UART

The RZ/V2N implements 10 channels Serial Communication Interface (RSCI) which supports various communication modes:

- UART
- Simple I2C

- Simple SPI

The RNX-RZV2N-SMARC exposes 4 UART interfaces as follows:

- SMARC SER0 connected to CPU SCIF0
- SMARC SER1 connected to CPU RSCI TXD0/RDX0 (CPU ports P50, P51)
- SMARC SER2 connected to CPU RSCI TXD1/RDX1/CTS1/RTS1 (CPU ports P52, P53, P62, P63)
- SMARC SER3 connected to CPU RSCI TXD2/RDX2 (CPU ports P54, P55)

The RZ/V2N RSCI in UART mode supports the following features:

- 32-stage FIFO registers for transmission and reception
- Data length: 7 to 9 bits
- Full-duplex and half-duplex communications
- Adjustable reception sampling timing from default timing
- Adjustable timing of transmission wave edge by register
- Selectable to low level or falling edge detection
- Digital noise filters included on signal paths from RXDn pin inputs

6.7 I2C

The RNX-RZV2N-SMARC provides five I²C bus interfaces on the SMARC connector.

I2C0 is available on the SMARC connector on the following pins:

- S48 / S49 – I2C_GP_CK / I2C_GP_DAT

I2C1 is available on the SMARC connector on the following pins:

- S5 / S7 – I2C_CAM0_CK / I2C_CAM0_DAT

I2C2 is available on the SMARC connector on the following pins:

- S1 / S2 - CSI1_TX+ / I2C_CAM1_CK / CSI1_TX- / I2C_CAM1_DAT

I2C3 is available on the SMARC connector on the following pins:

- S139 / S140 – I2C_LCD_CK / I2C_LCD_DAT

I2C6 is available on the SMARC connector on the following pins:

- P121 / P122 – I2C_PM_CK / I2C_PM_DAT

I2C8 is used internally to the PMIC and the PCIe clock generator and it is not available on the SMARC connector.

The following general features are supported by all I2C bus interfaces:

- Supports standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- Multimaster operation
- Master or Slave operation mode.

I2C usage table:

NAME	PERIPHERAL	ADDRESS
I2C8	PMIC RAA215300	(0x12<<1)+RW
	PCIe clock generator 9FGV0241AKLF	(0x6A<<1)+RW
I2C0	SMARC connector: I2C_GP	
I2C1	SMARC connector: I2C_CAM0	
I2C2	SMARC connector: I2C_CAM1	
I2C3	SMARC connector: I2C_LCD	
I2C6	SMARC connector: I2C_PM	

Figure 6.15: I2C usage and address table

6.8 SPI

Two SPI interfaces are accessible through the RNX-RZV2N-SMARC carrier board interface. The SPI interfaces are derived from RZ/V2N integrated synchronous serial interface (RSPI). Each instance of RSPI port can operate as either a master or as an SPI slave. The following features are supported:

- SPI serial communication (4-wire) and clock synchronous (3-wire)
- Transmit-only operation is available
- Receive-only operation is available
- Serial communication is possible in master mode and slave mode
- RSPCK polarity switching
- RSPCK phase switching
- Transfer bit length selectable from 4 to 32 bits
- 32 bit × 16 stage FIFO transmit and receive buffers
- Up to four frames transferable in one round of transmission or reception
- Byte swap operating function

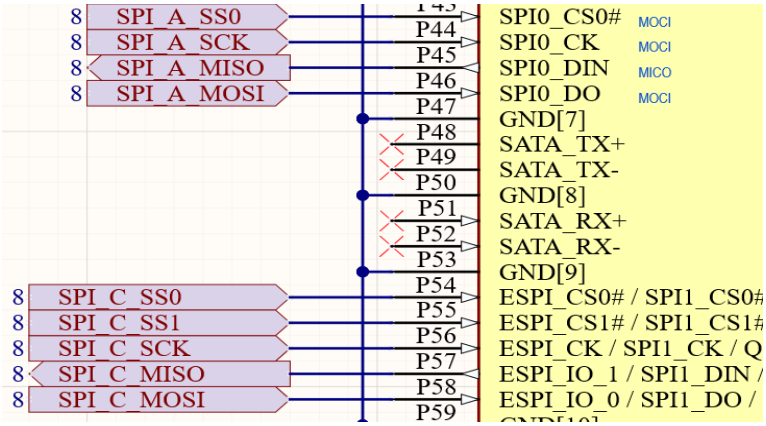

Figure 6.16: SPI on SMARC connector

6.9 CAN signals

The FlexCAN module is a communication controller implementing the CAN protocol according to the ISO 11898-1:2015 standard and CAN 2.0 B protocol specifications.

RNX-RZV2N-SMARC provides 2 CAN interfaces on the SMARC connector.

Figure 6.17: CAN signals on SMARC connector

6.10 GPIO

On the carrier board interface, 13 GPIOs are available, they are provided by the RZ/V2N SoC.

6.11 12-Bit A/D Converter

The RZ/V2N incorporates three units of 12-bit successive approximation A/D converter.

RNX-RZV2N-SMARC provides 8 channels on J3 (FFC, TE 1-2328702-0, 0.5mm pitch):

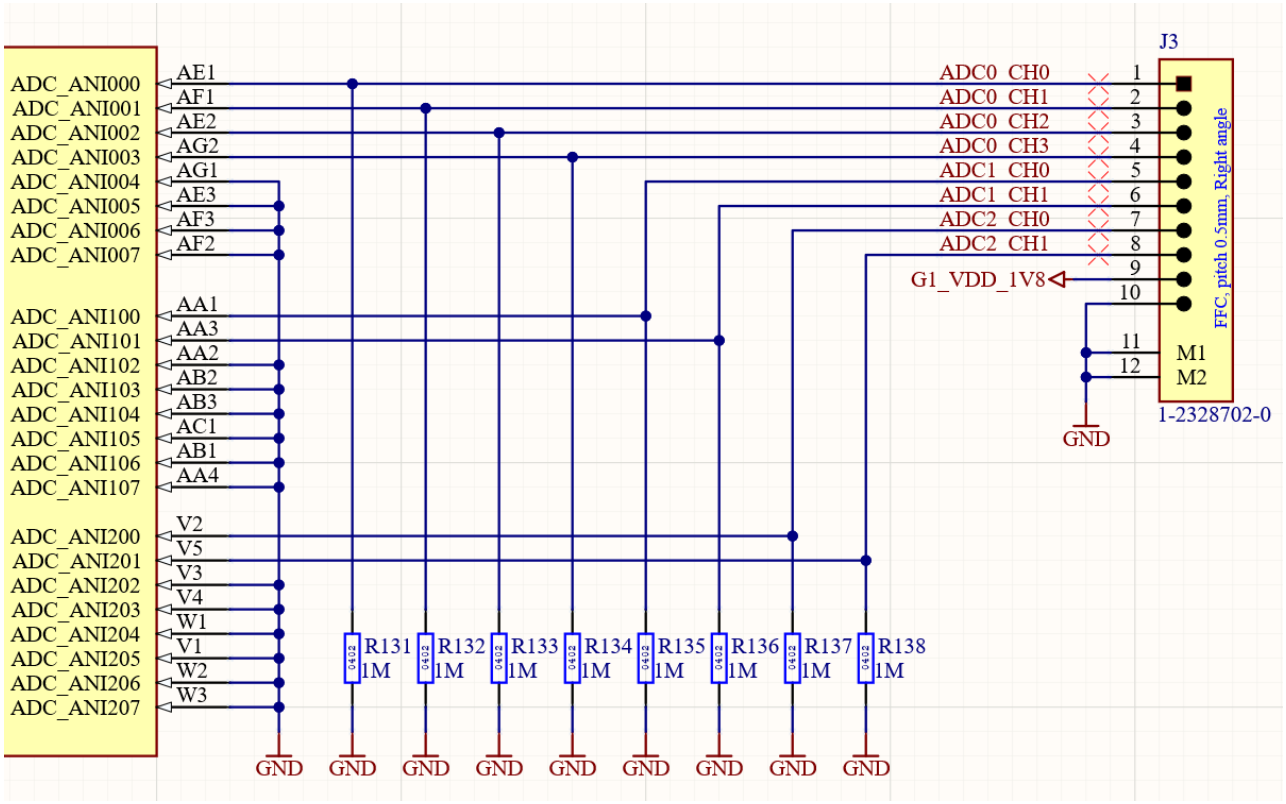

Figure 6.18: Analog inputs

6.12 PMIC Programming

The PMIC on SoM can be programmed via J5 (FFC, 0.5mm pitch).

For more information please contact Ronetix.

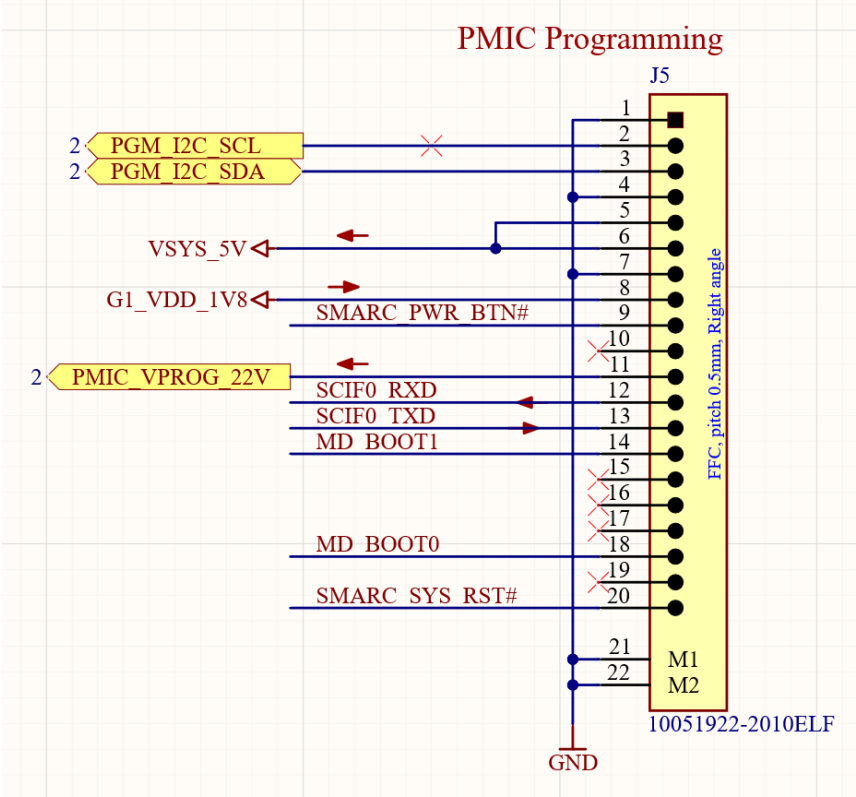

Figure 6.19: PMIC programming

6.13 JTAG

The System JTAG Controller (SJC) provides debug and test control with maximum security. The test access port (TAP) is designed to support features compatible with the IEEE standard 1149.1 v2001 (JTAG). Support IEEE P1149.6 extensions to the JTAG standard are for AC testing of selected IO signals. The JTAG signals are available on J2 (SM10B-SRSS-TB), 10-pin connector.

7. Power Supply

7.1 Power supply from base board

RNX-RZV2N-SMARC is powered by regulated DC supply 5.0V

Signal	Type	Description
VSYS_5V	Power input	Main Power Supply 5.0V
GND	Power input	Common ground

7.2 System Signals

Signal	Type	Description
PWR_BTB#	Input with Pull-Up resistor	ON/OFF button input (De-bouncing provided at this input). Short connection to GND in OFF mode causes internal power management state machine to change state to ON. In ON mode short connection to GND generates interrupt (intended to SW controllable power down). Long above ~5s connection to GND causes “forced” OFF.
SYS_RST#	Input	PMIC Reset signal

8. Electrical Specifications

8.1 Absolute maximum ratings

Parameter	Mln	Max	Unit
VSYS_5V – Main Power Supply	-0.5	5.5	V

8.2 Recommended Operating Conditions

Parameter	Mln	Typ	Max	Unit
VSYS_5V – Main Power Supply	4.75	5.0	5.25	V
VSYS_5V – recommended source capability		8.0		A

9. Operating Temperature Ranges

Range	Temp.
Commercial	0° to +70°C
Industrial	-40° to +85°C

10. Warranty Terms

Ronetix guarantees hardware products against defects in workmanship and material for a period of one (1) year from the date of shipment. Your sole remedy and Ronetix's sole liability shall be for Ronetix, at its sole discretion, to either repair or replace the defective hardware product at no charge or to refund the purchase price. Shipment costs in both directions are the responsibility of the customer. This warranty is void if the hardware product has been altered or damaged by accident, misuse or abuse.

Disclaimer of Warranty

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