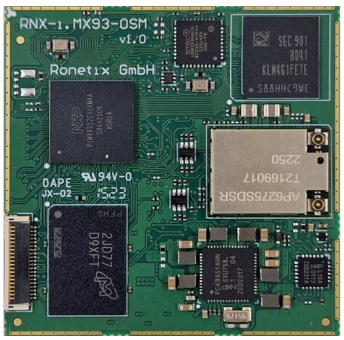
High-performance System on Module (SOM)

RNX-i.MX93-OSM

Open Standard Module with NXP i.MX93

Datasheet

rev 1.0



Ronetix Development Tools GmbH
Hirschstettner Str. 19/Z110
1220 Vienna
Austria
www.ronetix.at

1. Document Revision History

Revision	Date	Notes
1.0	30-Jun-2023	Initial release

2. Table of Contents

Table of Contents

3. Overview

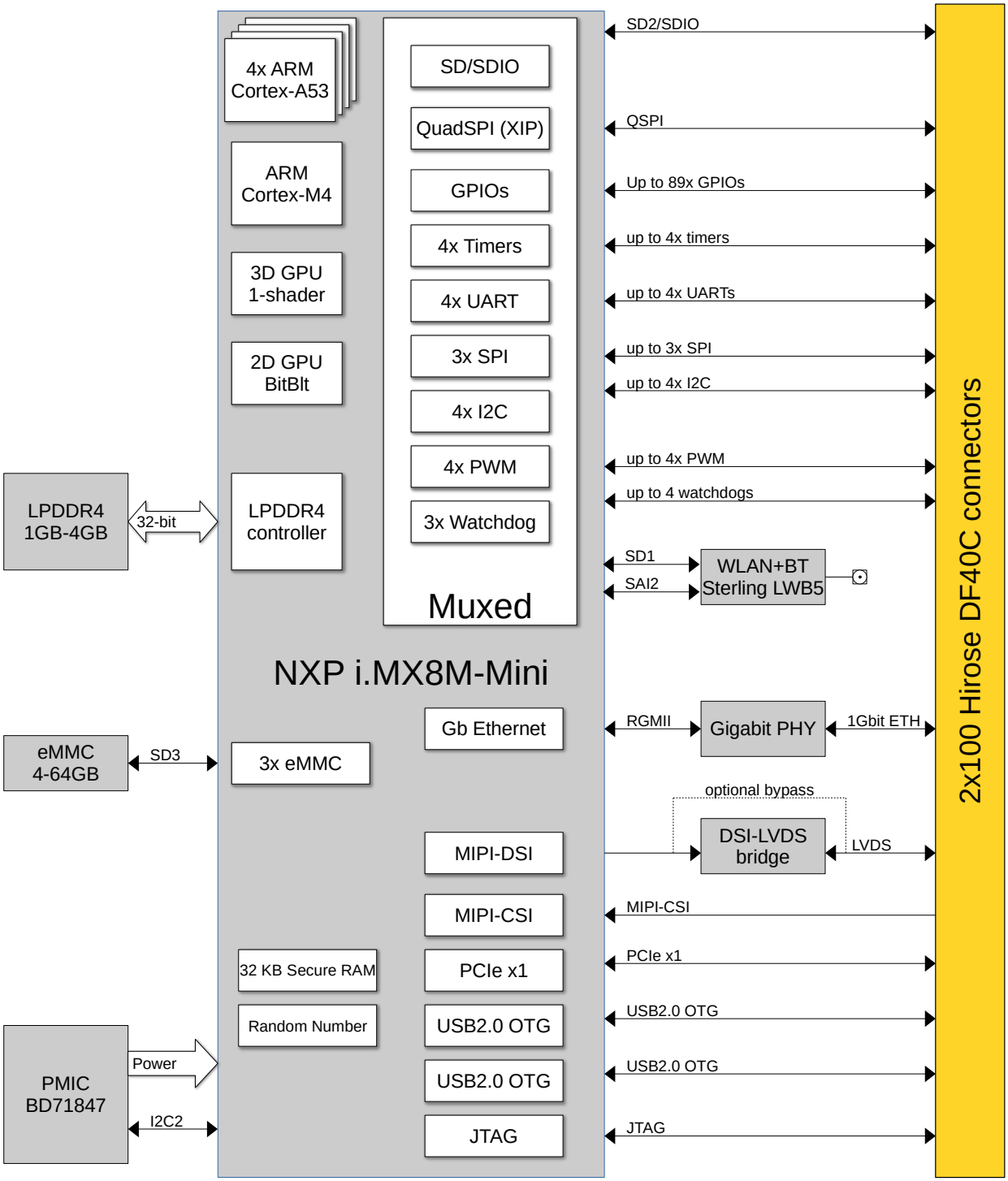
3.1 General Information

The **RNX-i.MX93-OSM** is a high-performance processing for low-power CPU Module (SoM – System On Module) that perfectly fits various embedded products of connected and portable devices. It is based on the NXP i.MX93 family of multipurpose processors from which feature a dual ARM® Cortex™-A55 up to 1.7GHz + an additional ARM Cortex-M33 at 250 MHz. This Heterogeneous Multicore Processing architecture enables the device to run an open operating system like Linux on the Cortex-A55 core and an RTOS like FreeRTOS™ on the Cortex-M33 core for time and security critical tasks.

3.2 Highlights

CPU	• Dual Armv8.2-A, 64-bit Cortex™-A55 Core, 1.7GHz • ARM® Cortex™-M33, 250MHz
Memory	• RAM: 1 GiB LPDDR4 (optional: up to 4 GiB) • eMMC: 4 GiB (optional: up to 64 GiB)
Display	• LVDS, 1366x768p60 or 1280x800, 60Hz • MIPI DSI, up to 1920x1200, 60Hz
Camera	• MIPI-CSI, 4 data lanes
Network	• Ethernet: 2x RGMII • WiFi: AP6275SDSR or AZ-CM276, 802.11ax/ac/a/b/g/n (optional) • Bluetooth: Bluetooth 5.3 (optional)
I/O	• 2 USB2.0 OTG ports or 1 USB2.0 OTG + 3 USB2.0 Host ports • • Up to 4x UART ports • MMC/SD/SDIO • Up to 2x SPI • Up to 2x I2C • Up to 4x general purpose PWM signals • 40x GPIOs
Electrical	• Supply Voltage: 5.0V
Physical	• Board size: Open Standard Module, Size-L, 45x45mm • Operation temperature: 0° +70°C, -20° to 85° C (optional) • Relative humidity: 10% to 90%

3.3 SoM Block Diagram



4. CPU Module Hardware Components

This chapter describes the hardware components of RNX-i.MX93-OSM SoM.

4.1 Power supply

RNX-iMX93-OSM uses NXP's PCA9541 as a Power Management Integrated circuit (PMIC) designed specifically for use with NXP's i.MX9 series of application processors. The PMIC regulates all power rails required on CPU module from a single 5.0V power supply.

The PMIC is fully programmable via the I2C interface and associated register map. Additional communication is provided by direct logic interfacing including interrupt, watchdog and reset.

4.2 CPU i.MX93

The i.MX 93 includes powerful dual Arm® Cortex®-A55 processors with speeds up to 1.7 GHz integrated with a NPU that accelerates machine learning inference. A general-purpose Arm® Cortex®-M33 running up to 250 MHz is for real-time and low-power processing. Robust control networks are possible via CAN-FD interface. Also, dual 1 Gbps Ethernet controllers, one supporting Time Sensitive Networking (TSN), drive gateway applications with low latency. The i.MX 93 industrial qualified part is particularly useful for applications such as:

• Industrial human machine interface (HMI)

• Industrial vision

• Scanning and printing

• EV Charging

• Industrial automation

• Touchless access control

• Energy meter

• Energy grid equipment

4.2.1 CPU Block Diagram

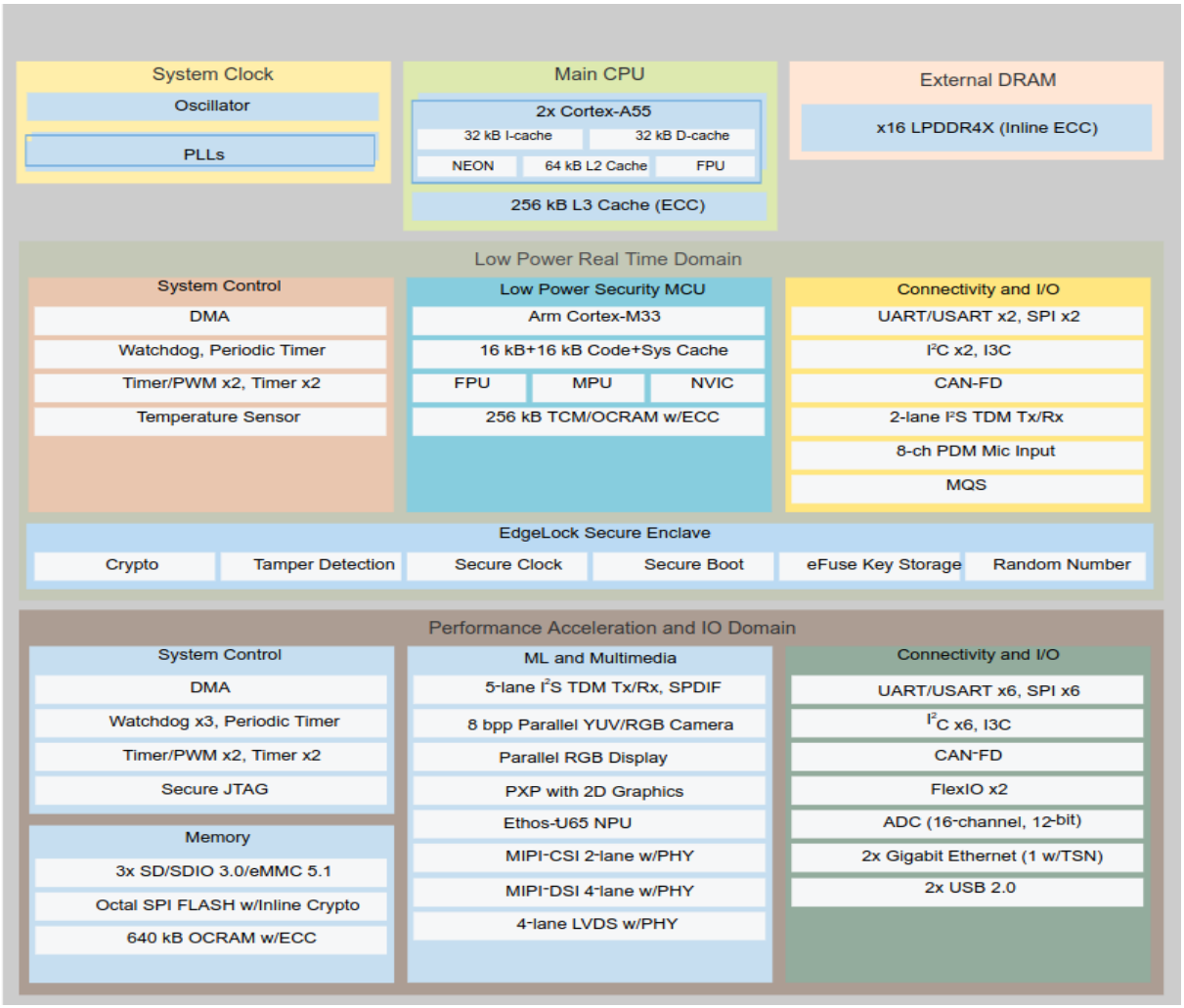


Figure 4.1: i.MX93 block diagram

4.2.2 CPU Platform

The i.MX93 processor implements two ARM® Cortex®-A55 cores intended for high level O/S, with an ARM® Cortex®-M33 core dedicated for real-time and security tasks.

The ARM Cortex-A55 platform has the following features:

- Dual ARM Cortex-A55 Cores
- Target frequency of 1.7GHz
- The core configuration is symmetric, where each core includes:

- 32 KByte L1 Instruction Cache
- 32 KByte L1 Data Cache
- 64 Kbyte per core L2 cache
- Media Processing Engine (MPE) with Arm® NeonTM technology supporting the Advanced Single Instruction Multiple Data architecture
- Floating Point Unit (FPU) with support of the Arm® VFPv4-D16 architecture
- 256kB shared cluster L3 cache
- Core cache protection (parity/ECC) supported

The ARM Cortex-M33 platform includes the following features:

- Microcontroller available both for boot and for customer application
- Cortex-M33 CPU core operating at 250 MHz
- 16KB L1 Instruction Cache
- 16KB L1 Data Cache
- 256 KByte TCM, also accessible as SRAM by the rest of the system
- ECC support for both cache and TCM

4.3 Memory

4.3.1 DRAM

RNX-iMX93-OSM is standard equipped with 1 GB LPDDR4 memory. Optionally up to 2 GB can be assembled. The data bus is 16-bit wide.

4.3.2 eMMC – non-volatile storage memory

RNX-iMX93-OSM is standard equipped with 4 GB eMMC. Optionally up to 32 GB can be assembled.

The eMMC can be used as boot device.

4.4 WLAN

RNX-iMX93-OSM optional wireless communication is implemented with SparkLAN **AP6275SDSR** LGA module. AP6275SDSR is an 802.11ax/ac/a/b/g/n WiFi + BT 5.3 Combo M.2 LGA Type 1216 Module (WiFi 6) with two external antenna connectors.

Instead of AP6275SDSR, RNX-i.MX93-OSM can be assembled with AzureWave **AW-CM276NF** LGA module. AW-CM276NF is an IEEE 802.11 ac/a/b/g/n WiFi + Bluetooth 5.0 complaint with Bluetooth 2.1+Enhanced Data Rate.

4.5 USB Hub

An optional USB Hub USB2534, connected to USB2, can be populated. In this case two additional USB ports (USBHUB2, USBHUB3) are available on the LGA contacts. USBHUB4 is connected to the WiFi.

4.6 GPIO Expander

An optional GPIO expander PCAL6416 can be populated. PCAL6416 is connected to I2C2 interface.

5. Open Standard Module LGA 662 contacts

The RNX-iMX93-OSM exposes on bottom side 662 LGA contacts.

6. CPU Module interfaces

6.1 Gigabit Ethernet

On RNX-iMX93-OSM the two RGMII 10/100/1000Mbps interfaces are available on LGA662 contacts.

- One Gigabit Ethernet controller with support for Energy Efficient Ethernet (EEE), Ethernet AVB, and IEEE 1588
- One Gigabit Ethernet controller with support for TSN in addition to EEE, Ethernet AVB, and IEEE 1588.

Both interfaces support the following main features:

- 10/100/1000 BASE-T IEEE 802.3 compliant.
- IEEE 802.3u compliant Auto-Negotiation.

- Supports all IEEE 1588 frames - inside the MAC.
- Automatic channel swap (ACS).
- Automatic MDI/MDIX crossover.
- Automatic polarity correction.
- Activity and speed indicator LED controls.

6.2 Display interfaces

RNX-iMX93-OSM provides the following display interfaces:

- MIPI DSI

  The MIPI-DSI interface is based on the four-lane MIPI display interface available with the iMX93 SoC. The DSI signals are available on the OSM LGA contacts.

  The chip support one 4-lane MIPI DSI display with pixels from the LCDIF. The key features of the MIPI DSI (controller and PHY) include:

  - Conforms to MIPI-DSI specification v1.2 and MIPI-DPHY specification v1.2
  - Maximum resolution limited to resolutions achievable with a 200MHz pixel clock and active pixel rate of 140Mpixel/s with
  - 24-bit RGB. This includes resolutions such as 1080p60 or 1920x1200p60
  - Support up to 4 Tx data lanes (plus 1 Tx clock lane)
  - Support 80Mbps - 1.5Gbps data rate per lane in high speed operation
  - Support 10Mbps data rate in low power operation

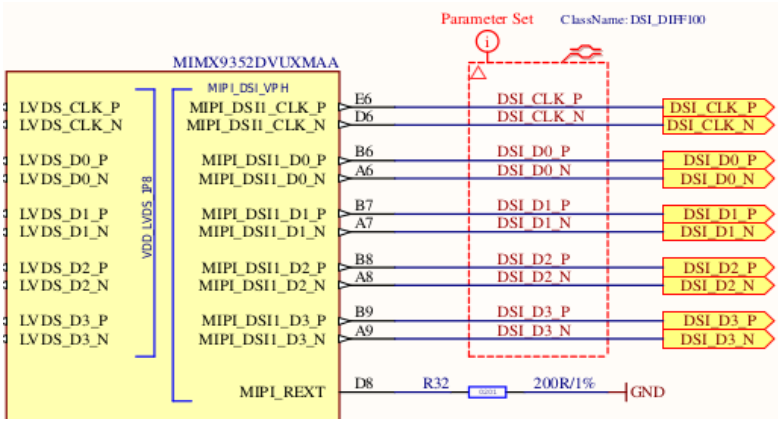


Figure 6.1: MIPI-DSI

- LVDS

  The LVDS interface is based on the four-lane LVDS display interface available with the iMX93 SoC. The LVDS signals are available on the OSM LGA contacts.

  The LVDS Display Bridge (LDB) connects to an External LVDS Display Interface. The purpose of the LDB is to support flow of synchronous RGB data to external display devices through the LVDS interface.

  - Supports FPD link
  - Supports single channel (4 lanes) output at up to 80MHz pixel clock and LVDS clock, with 7:1 ratio from LVDS data to pixel clock, implying up to 560Mbps LVDS data rate. This supports resolutions up to approximately 1366x768p60 or 1280x800p60.
  - Supports VESA and JEIDA pixel mapping
  - Supports LVDS Transmitter with four 7-bit channels. Each channel sends the 6 pixel bits and one control signal at 7 times the pixel clock rate. The data and control signals are transmitted over an LVDS link..

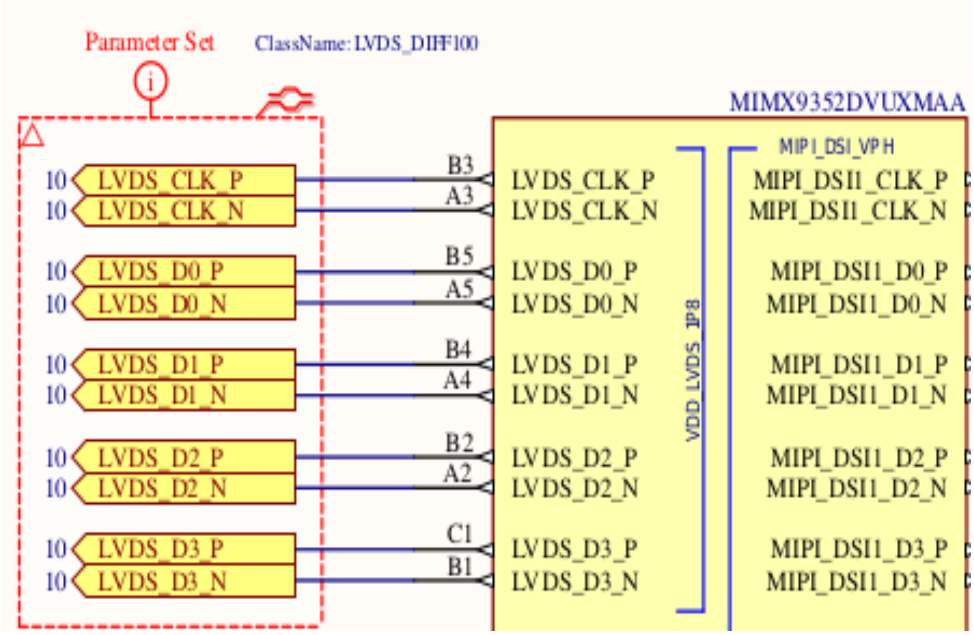


Figure 6.2: LVDS Interface

6.3 MIPI-CSI Camera interface

The MIPI-CSI interface is based on the four-lane MIPI camera interface available with the iMX93 SoC. The CSI signals are available on the OSM LGA contacts.

The MIPI Rx D-PHY includes the following features:

- Compliant to MIPI D-PHY interface specification, revision 1.2
- Lane operation ranging from 80 Mbps to 1.5 Gbps in forward direction
- Aggregate throughput up to 3 Gbps with two data lanes
- Maximum LP data rate supported of 10 Mbps
- PHY-Protocol Interface (PPI) for clock and data lanes
- Low-power Escape modes and Ultra Low Power state
- HS RX Equalizer up to 3dB
- Optional usage of external reference resistor (200 ohm)
- HS RX automatic offset cancellation

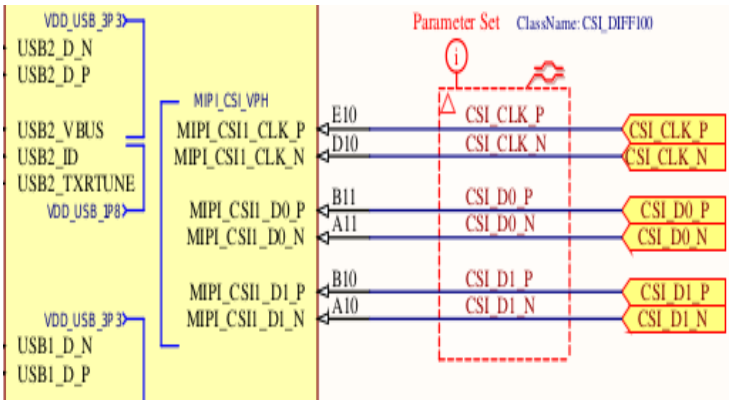


Figure 6.3: MIPI-CSI

6.4 USB interface

The i.MX93 SoC is equipped with two USB OTG controllers and PHYs. Each USB instance contains a USB 2.0 core. Both ports support dual-role functionality.

On RNX-i.MX93-OSM USB1 is available on the OSM LGA contacts. USB2 can be connected to the OSM LGA contacts or connected to a 4-port USB Hub. In the second case, USBHUB1, USBHUB2 and USBHUB3 are connected to the OSM LGA contacts, the USBHUB4 is connected to the WiFi LGA module.

The USB ports support the following main features:

- High-Speed/Full-Speed/Low-Speed OTG core
- Hardware support for OTG signaling, session request protocol, and host negotiation protocol
- up to 8 endpoints
- Low-power mode with local and remote wake-up capability

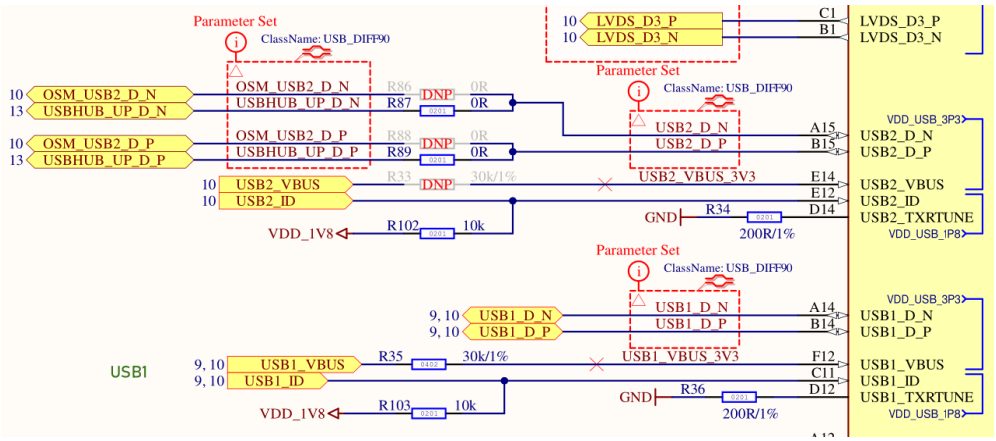


Figure 6.4: USB

6.5 MMC, SD, SDIO

The i.MX93 SoC is equipped with three MMC/SD/SDIO controller IPs (uSDHC). On RNX-iMX93-OSM SD1 is connected to the eMMC, SD3 can be connected to the WiFi module or to the LGA contacts, SD2 is available on the LGA contacts.

The uSDHC supports the following main features:

- Conforms to the SD Host Controller Standard Specification version 2.0/3.0
- Compatible with the eMMC System Specification version 4.2/4.3/4.4/4.41/4.5/5.0/5.1
- Compatible with the SD Memory Card Specification version 3.0 and supports the Extended Capacity SD Memory Card
- Card bus clock frequency up to 208 MHz
- Supports 1-bit/4-bit SD and SDIO modes, and 1-bit/4-bit/8-bit eMMC modes
- Supports single block/multi-block read and write
- Supports block sizes of 1 ~ 4096 bytes
- Embodies two fully configurable 256x32-bit FIFO for read/write data

6.6 UART

The RNX-iMX93-OSM exposes up to 4 UART interfaces some of which are multiplexed with other peripherals.

The i.MX93 UARTv2 supports the following features:

- High-speed TIA/EIA-232-F compatible
- 9-bit or Multidrop mode (RS-485) support
- 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none).
- Programmable baud rates up to 4 Mbps.
- 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud.
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s).
- Hardware flow control support for request to send and clear to send signals.
- RS-485 driver direction control.
- DCE/DTE capability.
- RX_DATA input and TX_DATA output can be inverted respectively in RS-232/RS-485 mode.
- Various asynchronous wake mechanisms with capability to wake the processor from STOP mode through an on-chip interrupt.

6.7 I2C

The i.MX93 SoC is equipped with eight I2C bus interfaces. I2C1 and I2C2 are available on the LGA contacts. I2C2 is used internally to the PMIC, GPIO Expander and USB Hub. The following general features are supported by all I2C bus interfaces:

- Compliant with Philips I2C specification version 2.1
- Supports standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- Multimaster operation
- Master or Slave operation mode.

I2C usage table:

I2C USAGE AND ADDRESS TABLE

NAME	PERIPHERAL	ADDRESS
I2C1 1.8V	i.MX93-OSM: OSM, LVDS	
I2C2 1.8V	i.MX93-OSM: PMIC control	(0x25<<1)+RW
	i.MX93-OSM: GPIO Expander, PCAL6416AHF	(0x20<<1)+RW
	i.MX93-OSM: USB Hub	

Figure 6.5: I2C address usage

6.8 SPI

Two SPI interfaces are accessible through the RNX-iMX93-OSM base board interface. The SPI interfaces are derived from i.MX93 integrated synchronous serial interface (eCSPI). Each instance of eCSPI port can operate as either a master or as an SPI slave. The following features are supported:

- Data rate up to 52 Mbit/s.
- Full-duplex synchronous serial interface.
- Master/Slave configurable.
- Up-to four chip select signals to support multiple peripherals.
- Transfer continuation function allows unlimited length data transfers.
- 32-bit wide by 64-entry FIFO for both transmit and receive data.
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable.
- Direct Memory Access (DMA) support.

6.9 PWM

Up to four PWM output signals are available at the RNX-iMX93-OSM base board interface. The following key features are supported:

- 16-bit up-counter with clock source selection
- 4 x 16 FIFO to minimize interrupt overhead
- 12-bit prescaler for division of clock
- Sound and melody generation
- Active high or active low configured output
- Interrupts at compare and rollover

6.10 GPIO

Up-to 40 of the i.MX93 general purpose input/output (GPIO) signals are available on the LGA contacts. When configured as an output, it is possible to write to an i.MX93 register to control the state driven on the output pin. When configured as an input, it is possible to detect the state of the input by reading the state of an i.MX93 register. In addition GPIOs peripheral can produce interrupts.

6.11 JTAG

The System JTAG Controller (SJC) provides debug and test control with maximum security. The test access port (TAP) is designed to support features compatible with the IEEE standard 1149.1 v2001 (JTAG). Support IEEE P1149.6 extensions to the JTAG standard are for AC testing of selected IO signals. The JTAG signals are available on the LGA contacts.

7. Power Supply

7.1 Power supply from base board

RNX-iMX93-OSM is powered by regulated DC supply 5.0V

Signal	Type	Description
VSYS_5V	Power input	Main Power Supply 5.0V
GND	Power input	Common ground

7.2 System Signals

Signal	Type	Description
PWR_BTB#	Input with Pull-Up resistor	ON/OFF button input (De-bouncing provided at this input). Short connection to GND in OFF mode causes internal power management state machine to change state to ON. In ON mode short connection to GND generates interrupt (intended to SW controllable power down). Long above ~5s connection to GND causes “forced” OFF.
SYS_RST#	Input	PMIC Reset signal

8. Electrical Specifications

8.1 Absolute maximum ratings

Parameter	Mln	Max	Unit
VSYS_5V – Main Power Supply	-0.5	5.5	V

8.2 Recommended Operating Conditions

Parameter	Mln	Typ	Max	Unit
VSYS_5V – Main Power Supply	4.75	5.0	5.25	V
VSYS_5V – recommended source capability		4.0		A

9. Operating Temperature Ranges

Range	Temp.
Commercial	0° to +70°C
Industrial	-40° to +85°C

10. Warranty Terms

Ronetix guarantees hardware products against defects in workmanship and material for a period of one (1) year from the date of shipment. Your sole remedy and Ronetix’s sole liability shall be for

Ronetix, at its sole discretion, to either repair or replace the defective hardware product at no charge or to refund the purchase price. Shipment costs in both directions are the responsibility of the customer. This warranty is void if the hardware product has been altered or damaged by accident, misuse or abuse.

Disclaimer of Warranty

THIS WARRANTY IS MADE IN LIEU OF ANY OTHER WARRANTY, WHETHER EXPRESSED, OR IMPLIED, OF MERCHANTABILITY, FITNESS FOR A SPECIFIC PURPOSE, NON-INFRINGEMENT OR THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION, EXCEPT THE WARRANTY EXPRESSLY STATED HEREIN. THE REMEDIES SET FORTH HEREIN SHALL BE THE SOLE AND EXCLUSIVE REMEDIES OF ANY PURCHASER WITH RESPECT TO ANY DEFECTIVE PRODUCT.

Limitation on Liability

UNDER NO CIRCUMSTANCES SHALL RONETIX BE LIABLE FOR ANY LOSS, DAMAGE OR EXPENSE SUFFERED OR INCURRED WITH RESPECT TO ANY DEFECTIVE PRODUCT. IN NO EVENT SHALL RONETIX BE LIABLE FOR ANY INCIDENTAL OR CONSEQUENTIAL DAMAGES THAT YOU MAY SUFFER DIRECTLY OR INDIRECTLY FROM USE OF ANY PRODUCT. BY ORDERING THE CPU MODULE, THE CUSTOMER APPROVES THAT THE RONETIX CPU MODULE, HARDWARE AND SOFTWARE, WAS THOROUGHLY TESTED AND HAS MET THE CUSTOMER'S REQUIREMENTS AND SPECIFICATIONS.