COVER PAGE

i.MX8MM-COMPACT-CM

Variant: MINI-Full

21.09.2021

SVN Revision: 1517

I2C USAGE AND ADDRESS TABLE

NAME	PERIPHERAL	ADDRESS
I2C1 1.8V	*i.MX8MM-COMPACT-MB: Camera on CSI1*	*(0x3C<<1)+RW*
	*i.MX8MM-COMPACT-MB: RTC clock, 3.3V**	*(0x50<<1)+RW*
	*i.MX8MM-COMPACT-MB: Audio Codec, 3.3V**	*(0x34<<1)+RW*
	i.MX8MM-COMPACT-MB: miniPCIEe Ref. Clock	*(0x6A<<1)+RW*
I2C2 1.8V only on CM	*i.MX8Mx-COMPACT-CM: PMIC control*	*(0x4B<<1)+RW*
	i.MX8Mx-COMPACT-CM: LVDS	*(0x2C<<1)+RW*
I2C3 1.8V	*i.MX8MM-COMPACT-MB: PCIe M.2*	

Note: 3.3V* - through voltage translator

DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes.

DESIGN NOTE:
Example text for critical design notes.

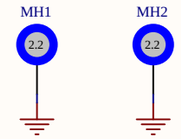
LAYOUT NOTE:
Example text for critical layout guidelines.

PCB1

PCB
Printed circuits board

PCB_iMX8MM-COMPACT-CM

Mounting Holes



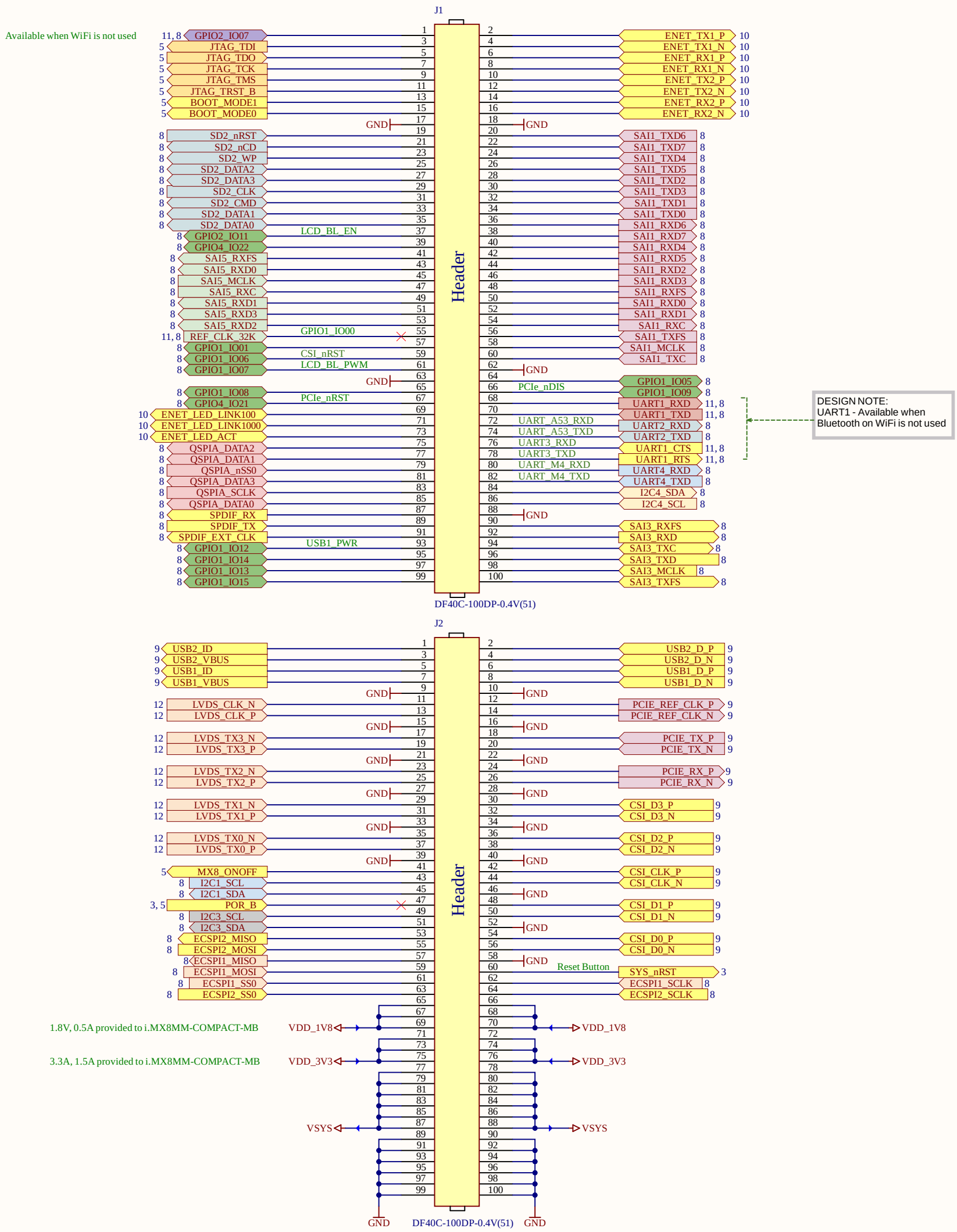
Mounting holes 5mm pad 2.2mm drill
BOARD MOUNTING HOLES - ONE IN EACH CORNER

Fiducials

FIDICIALS 3x TOP FIDICIALS 3x BOTTOM

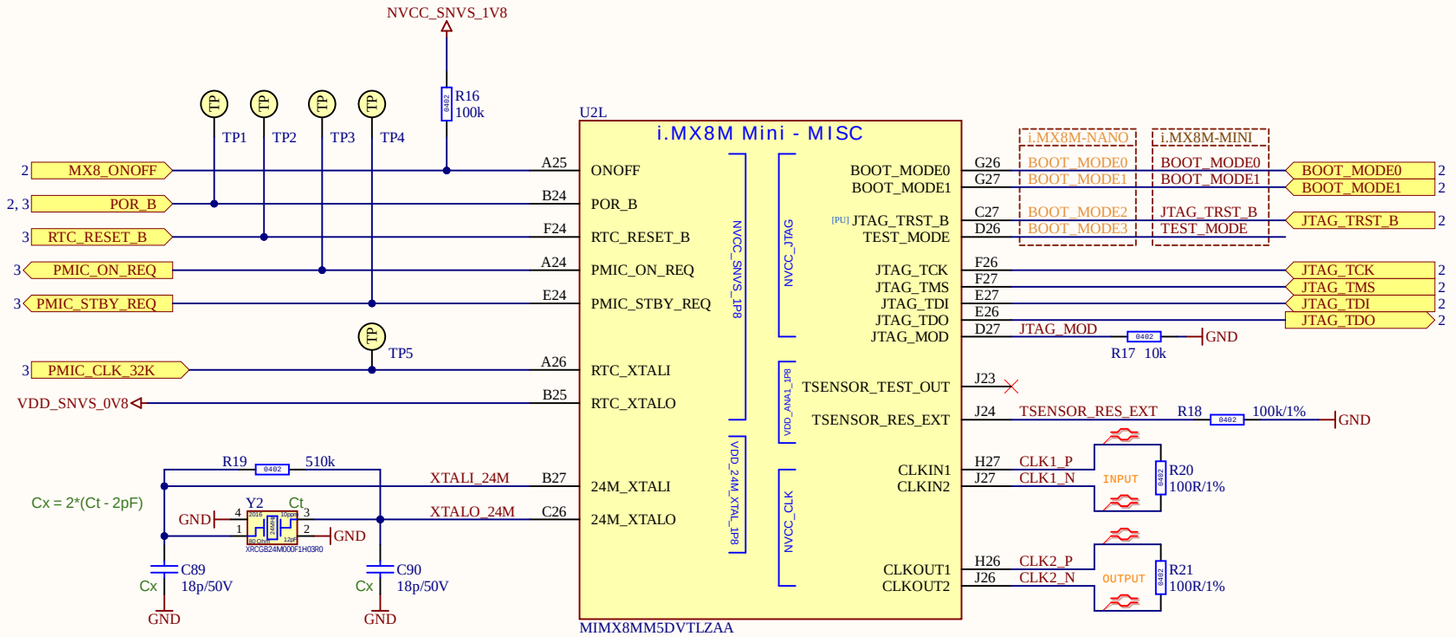
Title: COVER PAGE			Ronetix GmbH Hirschstettner Str. 19/Z110 1220 Vienna Austria
Size: A3	Number: 1	Revision: 1.0	
Date: 21.09.2021 Time: 17:15:02		Sheet 1 of 13	
File: 01_Title_Page.SchDoc			

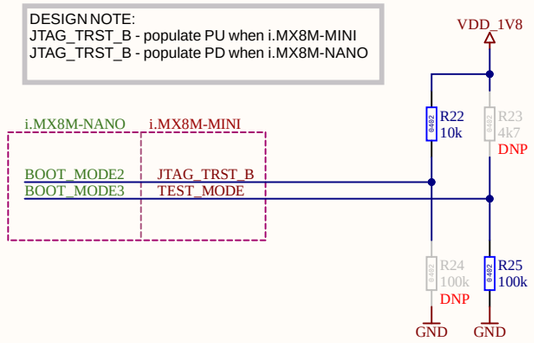
Hirose DF40C



Title	*Hirose DF40C*		*Ronetix GmbH* *Hirschstettner Str. 19/Z110* *1220 Vienna* *Austria*
Size: A3	Number: 2	Revision: 1.0	
Date: 21.09.2021	Time: 17:15:02	Sheet 2 of 13	
File: 02_Hirose_DF40C.SchDoc			

CPU Clocks, RESET

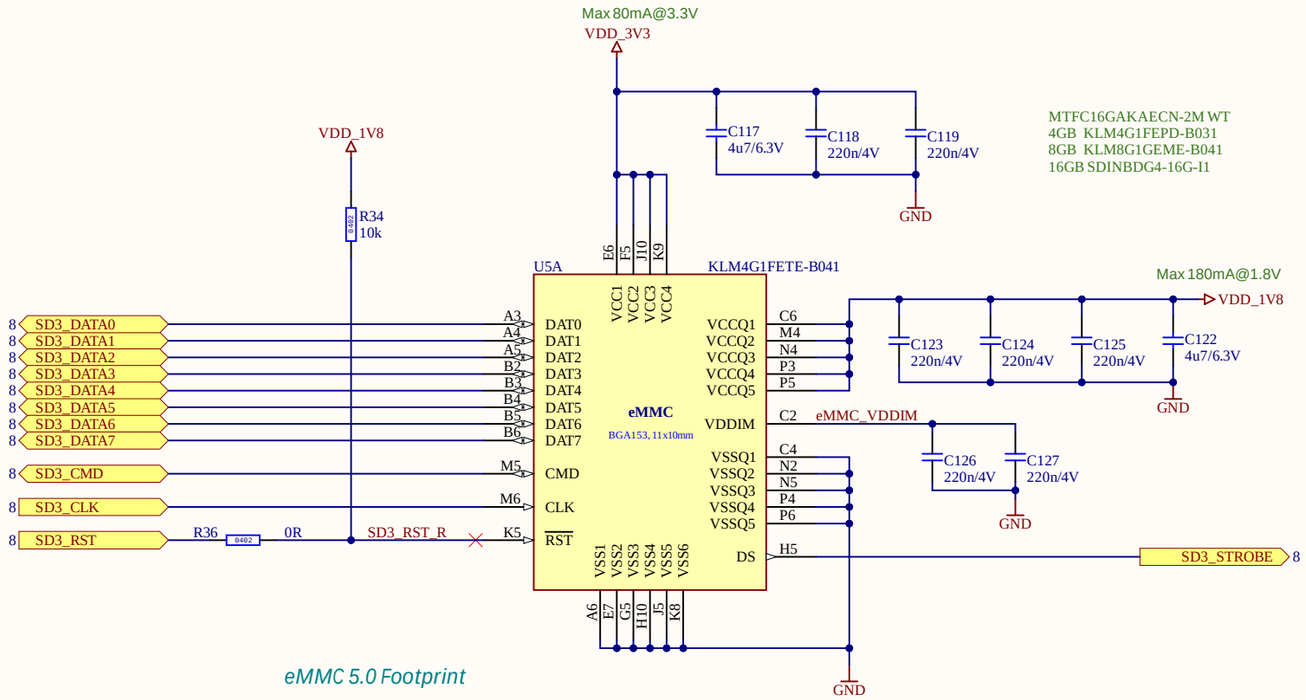


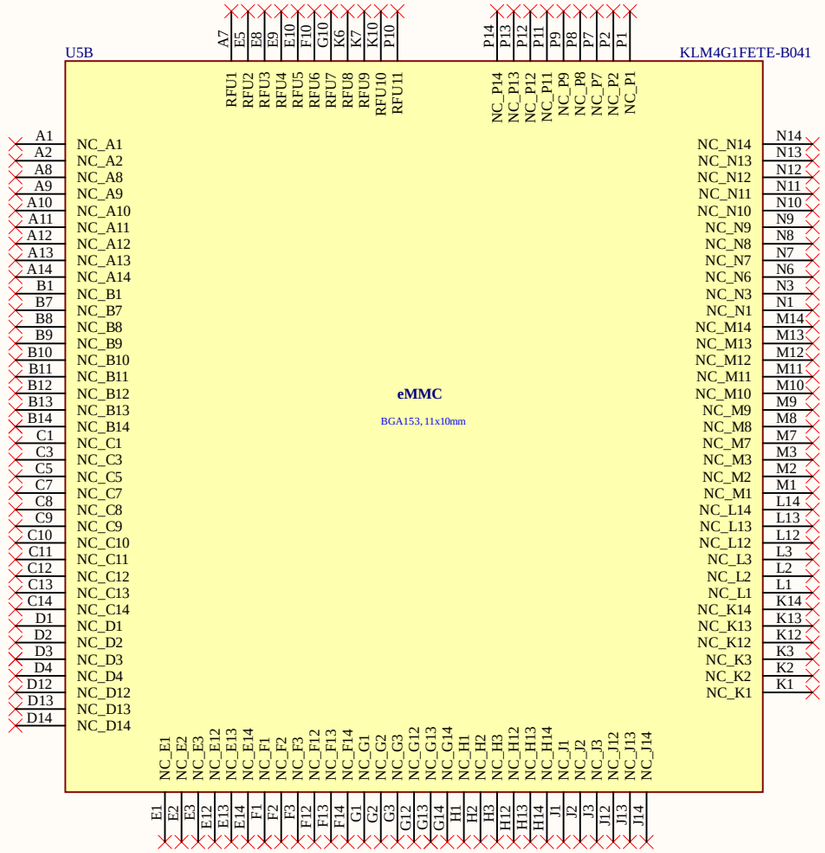


Title	*CPU Clocks, RESET*		*Ronetix GmbH*
Size: A3	Number: 5	Revision: 1.0	*Hirschstettner Str. 19/Z110*
Date: 21.09.2021	Time: 17:15:02	Sheet 5 of 13	*1220 Vienna*
File: 05_CPU_CLK_RST.SchDoc			*Austria*

RONETIX DEVELOPMENT TOOLS

eMMC

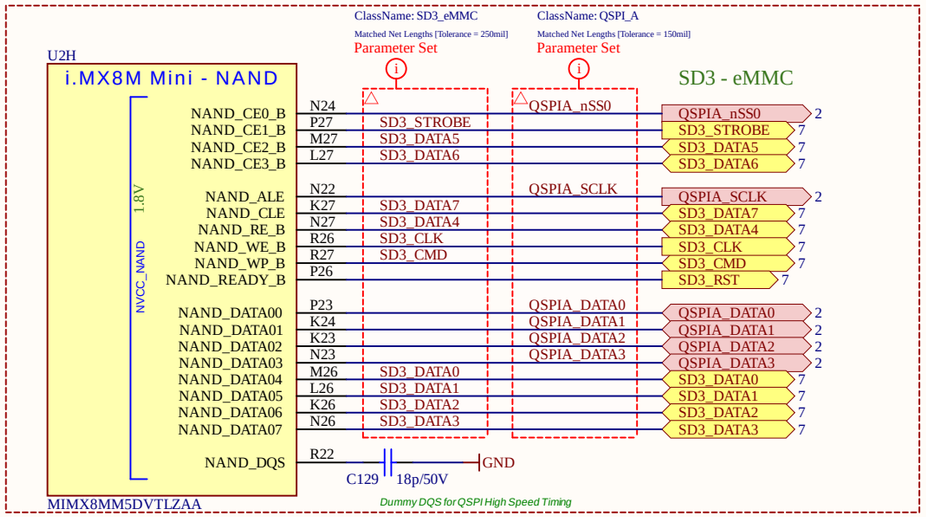


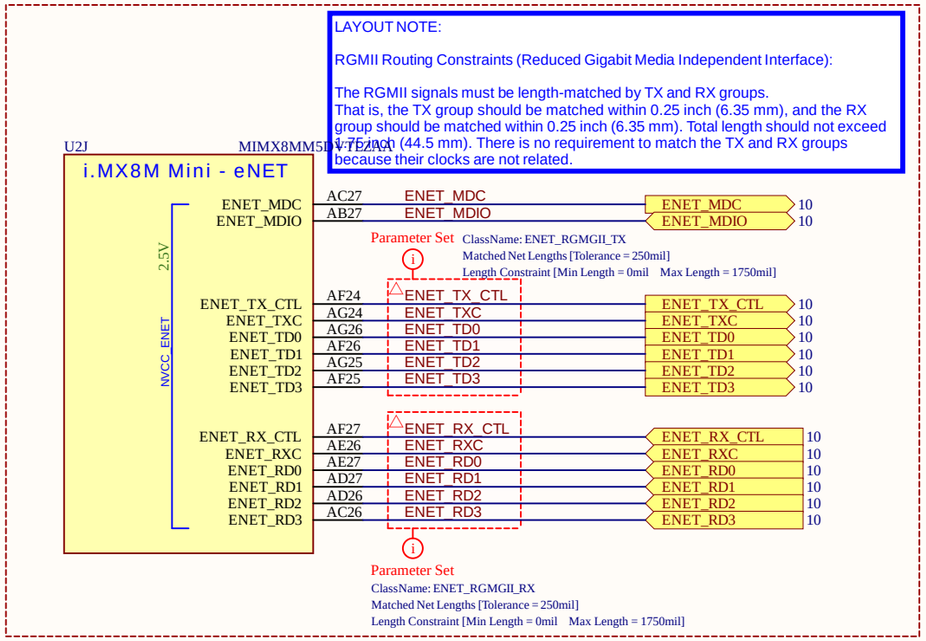


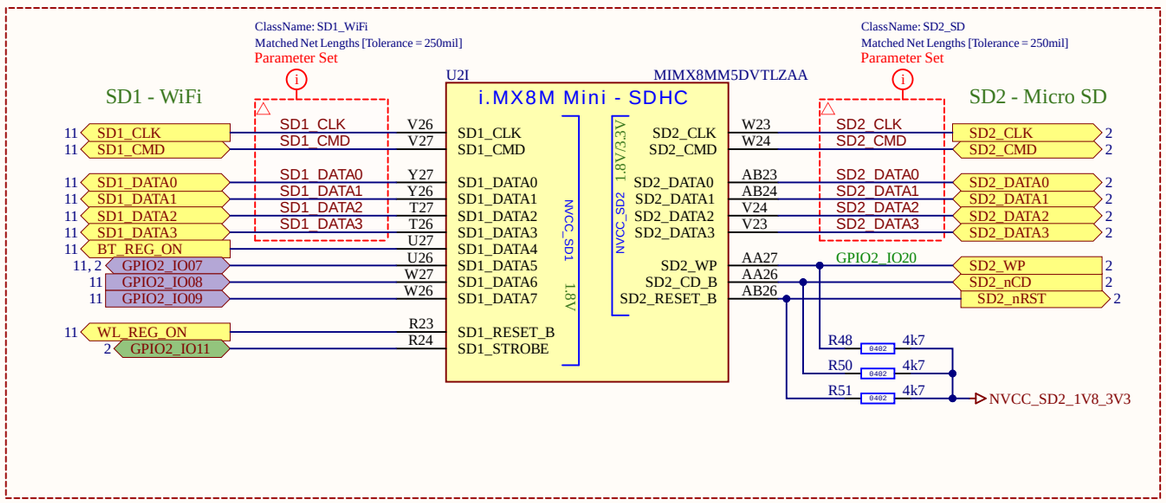
Title *eMMC*			*Ronetix GmbH*
Size: A3	Number: 7	Revision: 1.0	*Hirschstettner Str. 19/Z110*
Date: 21.09.2021	Time: 17:15:02	Sheet 7 of 13	*1220 Vienna*
File: 07_EMMC_QSPI.SchDoc			*Austria*

RONETIX DEVELOPMENT TOOLS

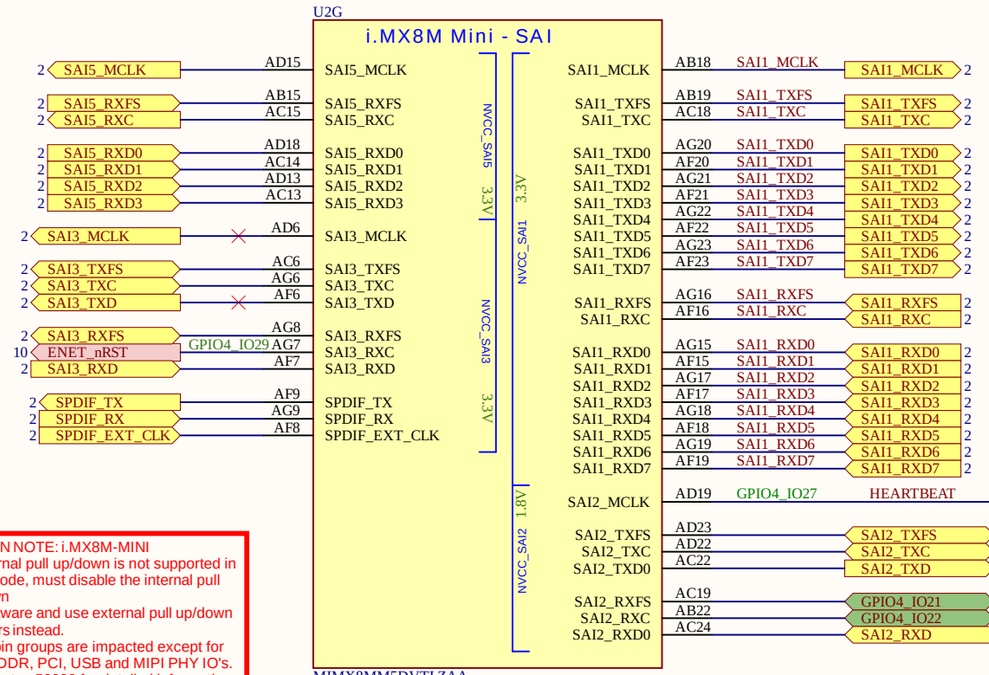
CPU - IO

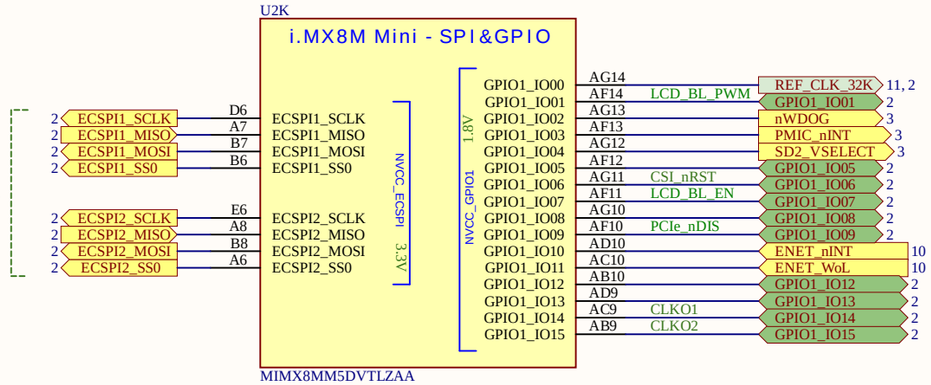


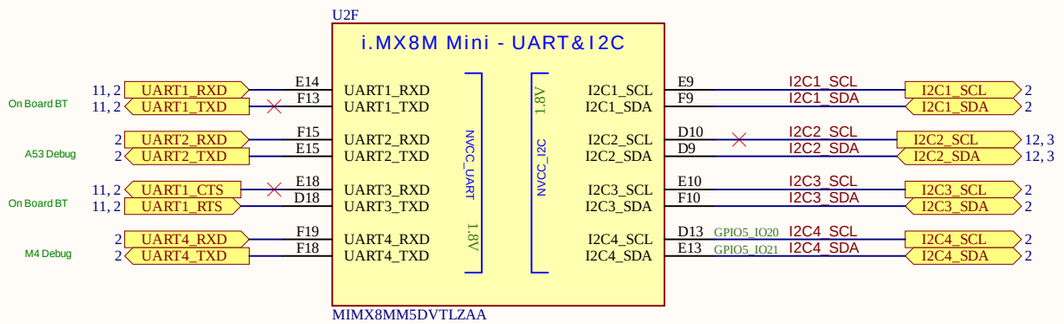


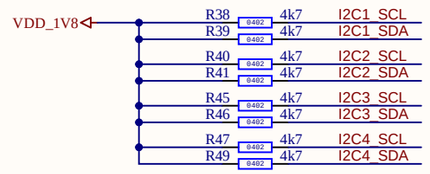


DESIGN NOTE: i.MX8M-MINI
IO internal pull up/down is not supported in 3.3V mode, must disable the internal pull up/down
via software and use external pull up/down resistors instead.
All IO pin groups are impacted except for XTAL, DDR, PCI, USB and MIPI PHY IO's.
See Errata e50080 for detailed information.
i.MX8M and i.MX8M-NANO are not affected.



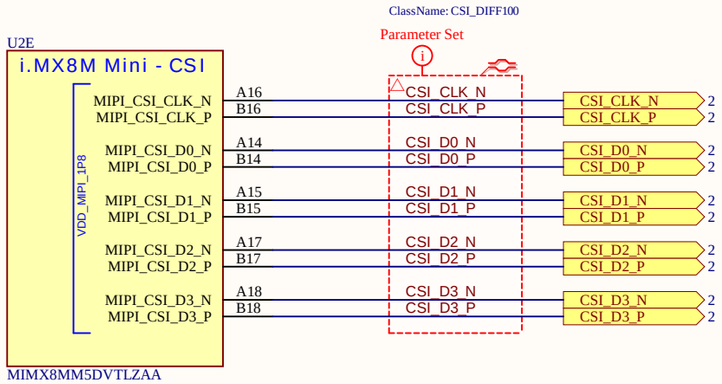


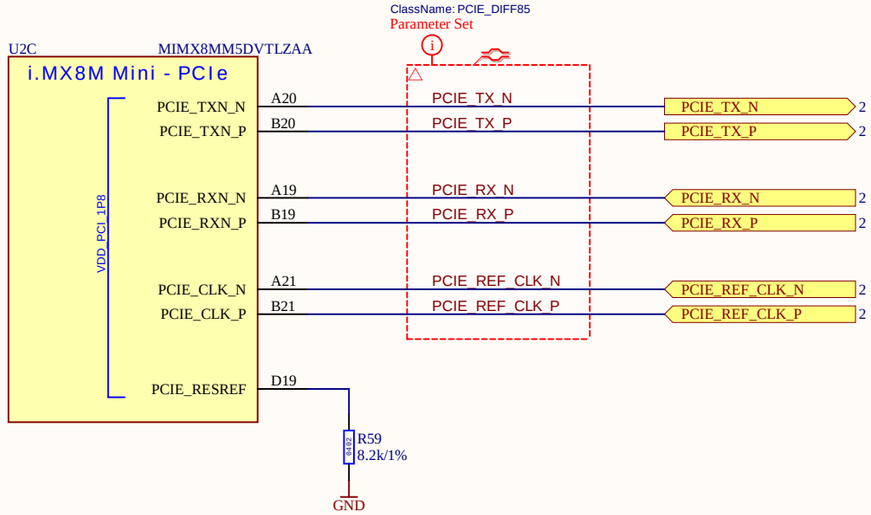




Title: CPU - IO			Ronetix GmbH Hirschstettner Str. 19/Z110 1220 Vienna Austria
Size: A3	Number: 8	Revision: 1.0	
Date: 21.09.2021 Time: 17:15:02	Sheet 8 of 13		
File: 08_CPU_IO.SchDoc			

CPU - PCIe, USB, DSI, CSI





Title	CPU - PCIe, USB, DSI, CSI		Ronetix GmbH Hirschstettner Str. 19/Z110 1220 Vienna Austria
Size: A3	Number: 9	Revision: 1.0	
Date: 21.09.2021	Time: 17:15:03	Sheet 9 of 13	
File: 09_CPU_PHY.SchDoc			

Ethernet

DESIGN NOTE:
Software MUST configure PHY
RGMII port for 2.5V operation.
Default = 1.5 V.

ClassName: ENET_DIFF100
Parameter Set

U8

ENET_TD0 ENET_TD1 ENET_TD2 ENET_TD3 ENET_TXC ENET_TX_CTL
ENET_RD0 ENET_RD1 ENET_RD2 ENET_RD3 ENET_RXC ENET_RX_CTL
2.5V
3.3V
ENET_MDC ENET_MDIO ENET_nRST

TXD0 TXD1 TXD2 TXD3 GTX_CLK TX_EN
RXD0/PHYAD0 RXD1/PHYAD1 RXD2/MODE1 RXD3/MODE3 RX_CLK/MODE2 RX_DV/MODE0
CLK_25M PPS
MDC MDIO RESET_N
XI [25MHz, 15pF] [30 ppm] [ESR 50Ohm]
XO
RBIAS [2.37k]
WOL_INT [OD]
INT [OD]
SIP SIN SOP SON
SD
VDD33
AVDD33 [63.8mA max]

TXRXP_A TXRXN_A TXRXP_B TXRXN_B TXRXP_C TXRXN_C TXRXP_D TXRXN_D
LED_ACT/PHYAD2 LED_LINK10_100 LED_LINK1000
VDDH
VDDH_REG 2.5V
2.5V (3.3V tolerant)
VDDIO_REG 1.5V or 1.8V
AVDDL1 AVDDL2 AVDDL3 AVDDL4 [50.8mA max]
1.1V
LX
1.1V DVDDL [113.7mA max]
GND

AR8031-AL1A

ENET_TX1_P ENET_TX1_N ENET_RX1_P ENET_RX1_N ENET_TX2_P ENET_TX2_N ENET_RX2_P ENET_RX2_N
ENET_LED_ACT ENET_LED_LINK1000

R64 10k 0402 — VDD_3V3
C135 18p/50V Cx — GND
Y3 Ct — XRCGB25M000F1H02R0 — Cx = 2*(Ct - 2pF)
C140 18p/50V Cx
R65 2.37k/1% 0402
ENET_WoL ENET_nINT
R66 10k 0402 — ENET_DVDDL_1V1
L9 0402 120R/0A50 - BLM15AG121SN1D — VDD_3V3
C130 220n/4V
C131 1uF/10V
C146 1uF/10V
C132 220n/4V
C133 1uF/10V
C134 220n/4V
NVCC_ENET to CPU
L7 0402 120R/0A50 - BLM15AG121SN1D
C136 220n/4V
C137 220n/4V
C138 220n/4V
C139 220n/4V
L8 4.7uH/0.6A - MBKK2012T4R7M
C142 220n/4V
C141 10u/6.3V
ENET_DVDDL_1V1

DESIGN NOTE:
Default Ethernet strapping options:
PHYAD2-0: PHY address 0x0
MODE3-0: RGMII mode (10/100/1000 half/full duplex)

NVCC_ENET
2k2 R67 2k2 R68
ENET_MDC
ENET_MDIO

ENET_RD0 PHYAD0
ENET_RD1 PHYAD1
ENET_LED_ACT PHYAD2
ENET_RD3 MODE3
ENET_RXC MODE2
ENET_RD2 MODE1
ENET_RX_CTL MODE0
ENET_LED_LINK1000 INT_SELECT

R69 1k R70 10k R71 10k R72 10k R73 10k R74 10k R75 10k R76 10k

Title	Ethernet		
Size: A3	Number: 10	Revision: 1.0	
Date: 21.09.2021	Time: 17:15:03	Sheet 10 of 13	
File: 10_ETHERNET.SchDoc			

Ronetix GmbH
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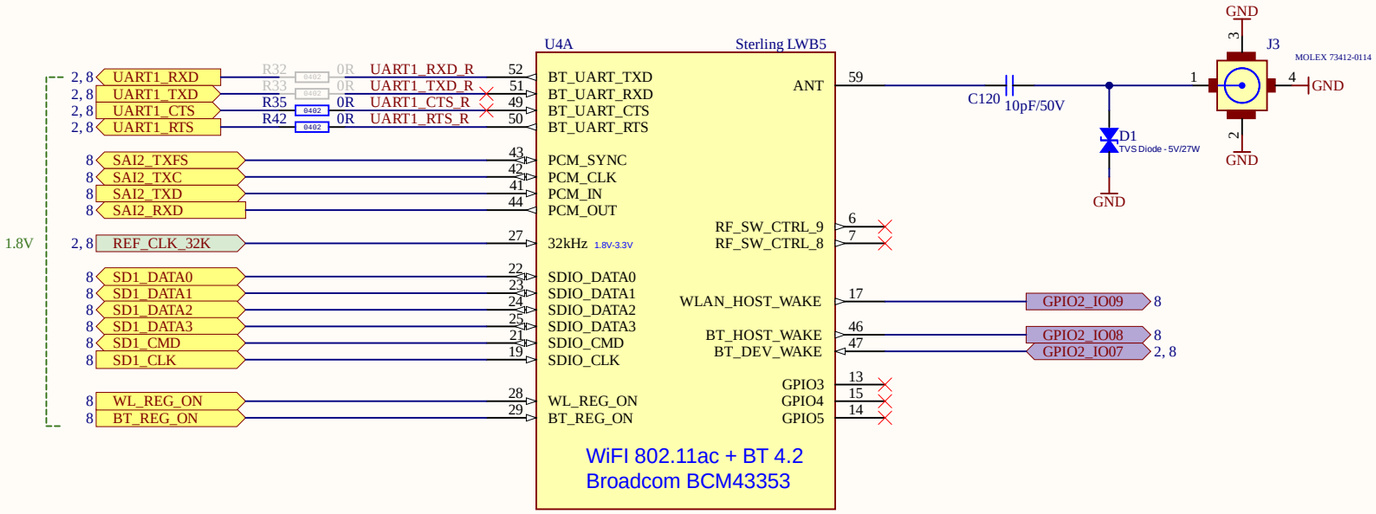
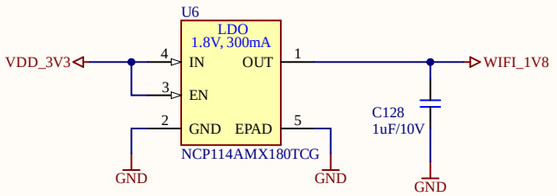
Austria

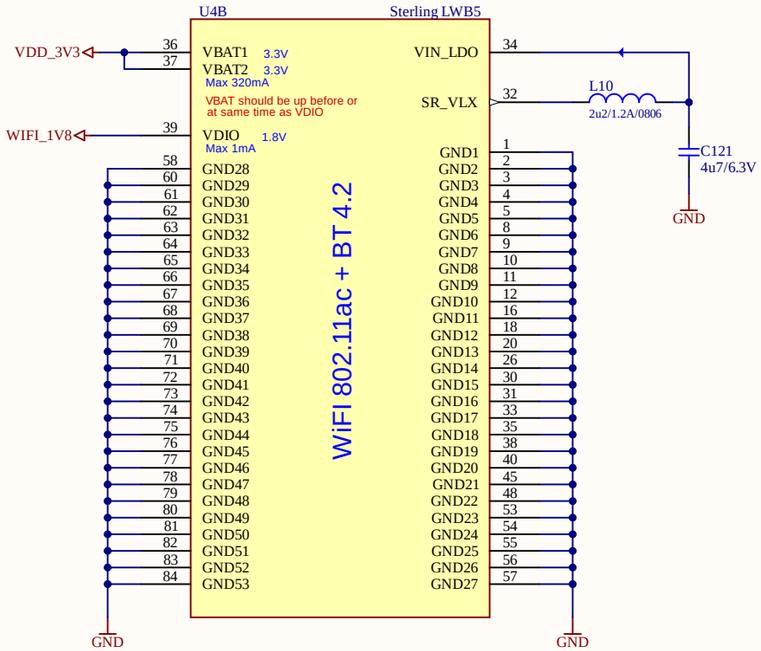
RONETIX DEVELOPMENT TOOLS

WiFi + Bluetooth





DESIGN NOTE:
The PMIC generates VDD_3V3 4-5mS after VDD_1V8 which doesn't match the WiFi module requirements.
Because of this the WIFI_1V8 is generated from VDD_3V3 using a LDO.

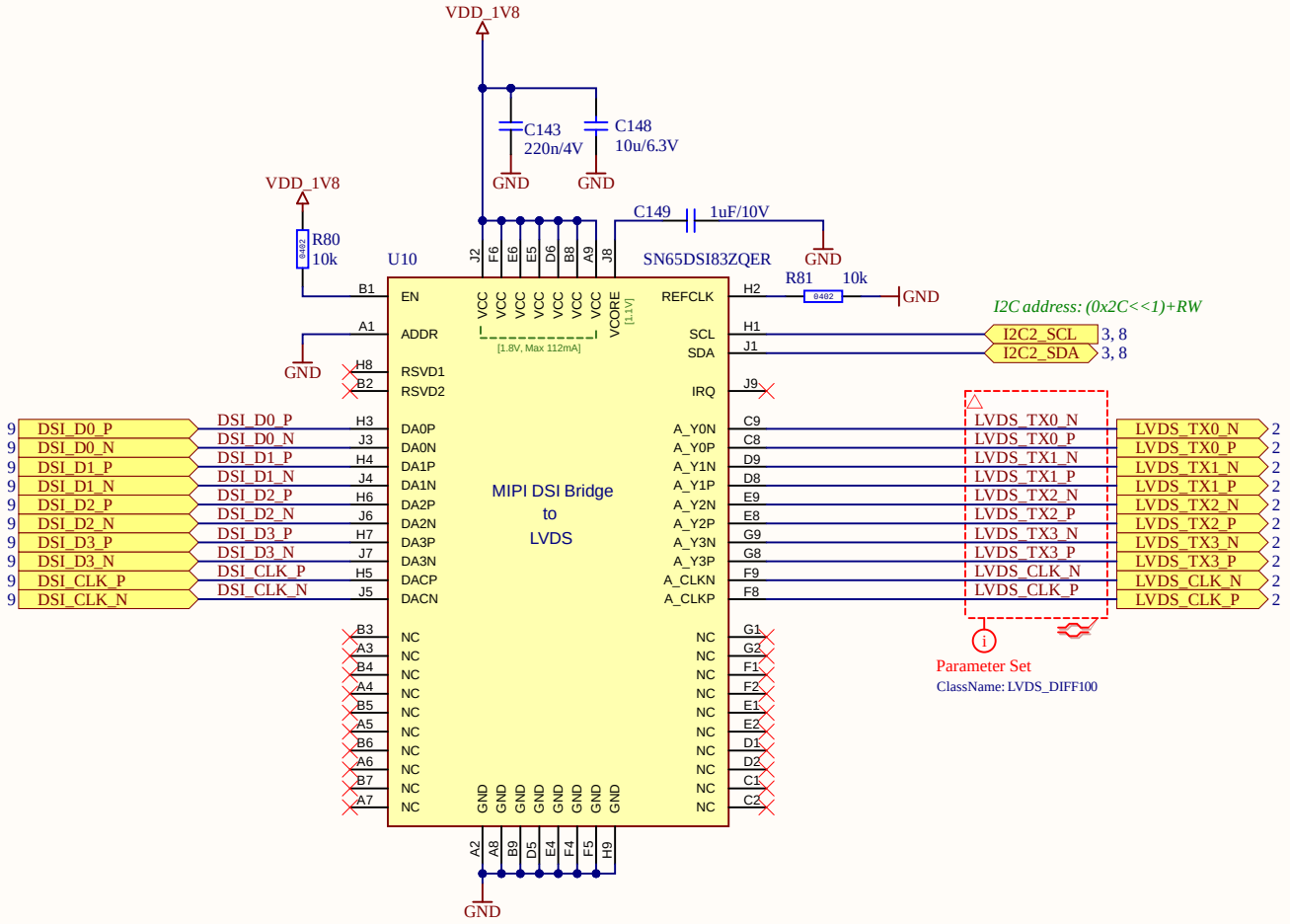


Title	***WiFi + Bluetooth***		*Ronetix GmbH*
Size: A3	Number: 11	Revision: 1.0	*Hirschstettner Str. 19/Z110*
Date: 21.09.2021	Time: 17:15:03	Sheet 11 of 13	*1220 Vienna*
File: 11_WiFi_BT.SchDoc			*Austria*

RONETIX DEVELOPMENT TOOLS

LVDS LCD Interface

Single-Channel DSI to Single-Link LVDS Bridge



Bypass DSI to LVDS converter

DSI_D0_P	R82	0R	DNP	LVDS_TX0_N
DSI_D0_N	R83	0R	DNP	LVDS_TX0_P
DSI_D1_P	R84	0R	DNP	LVDS_TX1_N
DSI_D1_N	R85	0R	DNP	LVDS_TX1_P
DSI_D2_P	R86	0R	DNP	LVDS_TX2_N
DSI_D2_N	R87	0R	DNP	LVDS_TX2_P
DSI_D3_P	R88	0R	DNP	LVDS_TX3_N
DSI_D3_N	R89	0R	DNP	LVDS_TX3_P
DSI_CLK_P	R90	0R	DNP	LVDS_CLK_N
DSI_CLK_N	R91	0R	DNP	LVDS_CLK_P

Title	*LVDS LCD Interface*		*Ronetix GmbH*
Size: A4	Number: 12	Revision: 1.0	*Hirschstettner Str. 19/Z110*
Date: 21.09.2021	Time: 17:15:03	Sheet 12 of 13	*1220 Vienna*
File: 12_LVDS.SchDoc			*Austria*

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