RONETIX

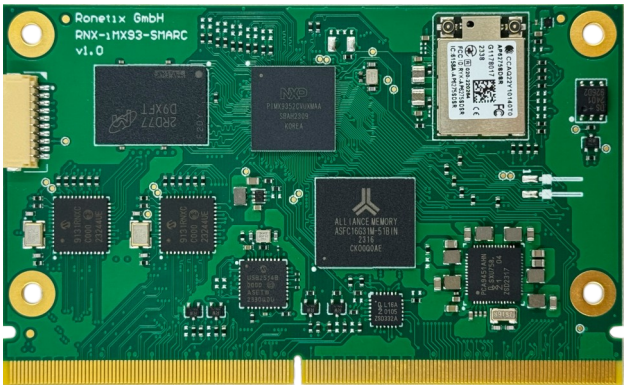
High-performance System on Module (SOM)

RNX-iMX93-SMARC

SMARC Module with NXP i.MX93

Datasheet

rev 1.1



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1. Document Revision History

Revision	Date	Notes
1.0	27-Jan-2024	Initial release
1.1	04-Nov-2026	Updated for hardware revision 1.2 (schematic variant A1-Full-AP6275SDSR): corrected PMIC (PCA9451A), DRAM (2 GiB LPDDR4X), MIPI-CSI (2 lanes), USB hub (USB2514B), Wi-Fi vendor, CPU debug/SPI/UART/I2C controller descriptions and company address. Added power rails, boot mode, SMARC pin assignment, UART, GPIO, audio and JTAG connector tables.

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3. Overview

3.1 General Information

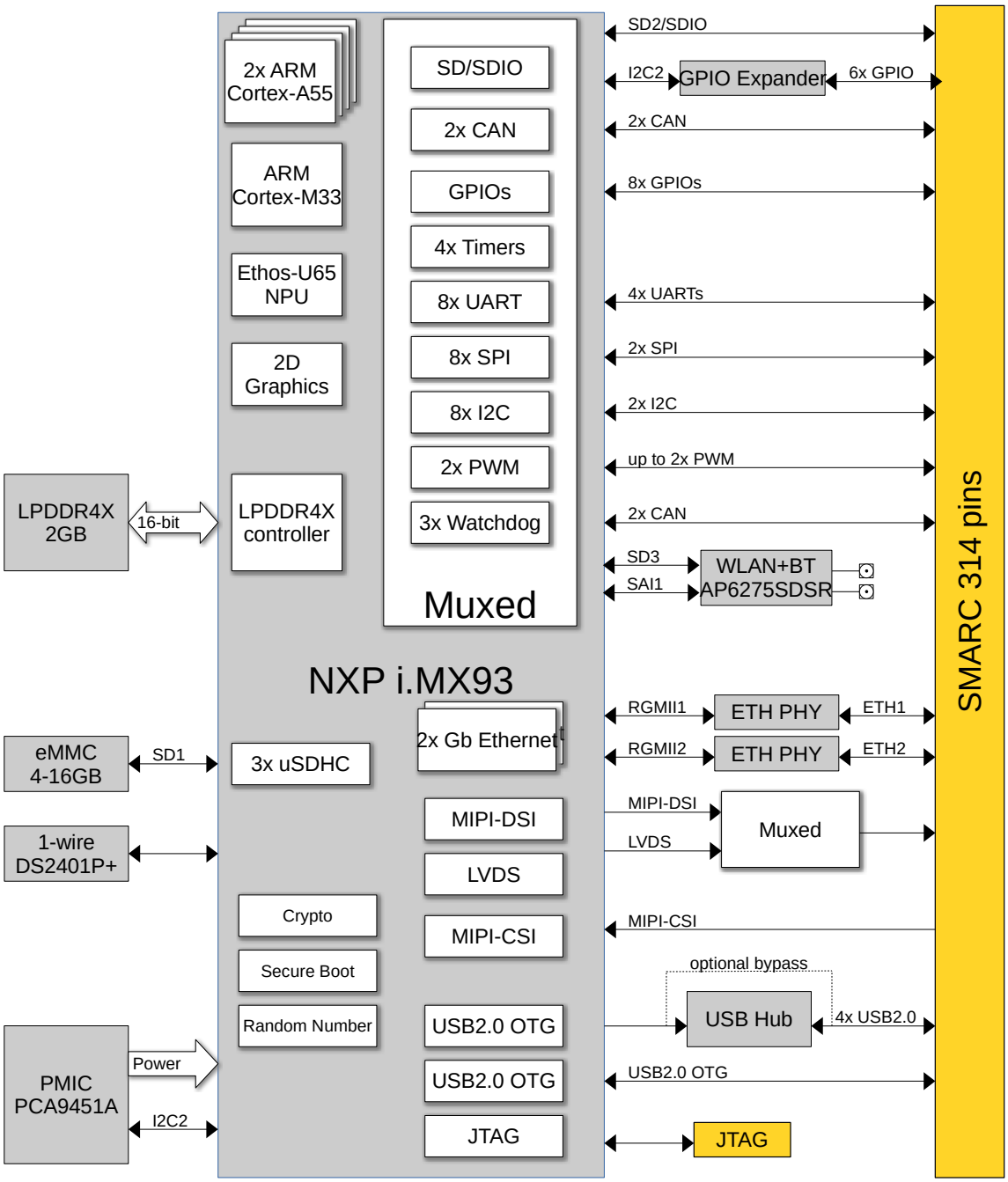
The RNX-iMX93-SMARC is a compact, low-power System on Module (SoM) in the SMARC 2.1 form factor (82 x 50 mm) for connected, portable and industrial embedded devices. It is based on the NXP i.MX 93 applications processor (i.MX 9352) with two Arm® Cortex®-A55 cores running at up to 1.7 GHz, an Arm® Cortex®-M33 real-time core at 250 MHz and an Arm® Ethos™-U65 microNPU for machine-learning inference. This heterogeneous multicore architecture allows an open operating system such as Linux to run on the Cortex-A55 cores while an RTOS such as FreeRTOS™ or Zephyr runs on the Cortex-M33 for time- and security-critical tasks.

This document describes hardware revision 1.2 of the module. The module is compliant with the SMARC specification v2.1.1. Where assembly options exist, the configuration of the standard (Full) variant is described and the alternatives are noted.

3.2 Highlights

CPU	• Dual Arm® Cortex®-A55 (Armv8.2-A, 64-bit), up to 1.7 GHz • Arm® Cortex®-M33, 250 MHz • Arm® Ethos™-U65 microNPU, EdgeLock® Secure Enclave
Memory	• RAM: 2 GiB LPDDR4X, 16-bit (other sizes on request) • eMMC 5.1: 4 GiB (optional: 16 GiB)
Display	• LVDS, single channel 4 lanes, up to 1366x768p60 or 1280x800p60 • MIPI DSI, 4 lanes, up to 1920x1200p60 (assembly option, shares pins with LVDS)
Camera	• MIPI CSI-2, 2 data lanes
Network	• Ethernet: 2x 10/100/1000 Mbps (KSZ9131RNX PHYs), one with TSN • Wi-Fi 6: AMPAK AP6275SDSR, 802.11ax/ac/a/b/g/n (optional) • Bluetooth 5.0 (optional, with the Wi-Fi module)
I/O	• 1x USB 2.0 OTG + 4x USB 2.0 Host (on-module hub) or 2x USB 2.0 without hub • 2x CAN FD • 4x UART (2 with RTS/CTS) • 1x SD/SDIO, 4-bit, 1.8 V / 3.3 V • 2x SPI • 2x I2C (I2C_PM and I2C_GP/I2C_CAM0/I2C_LCD) • 1x I2S audio (SAI3) • Up to 2x PWM (GPIO5/PWM_OUT, LCD0_BKLT_PWM) • 14x GPIOs (8 from i.MX 93, 6 from the I2C GPIO expander) • JTAG / SWD debug connector
Electrical	• Supply voltage: 5.0 V ±5% (VDD_IN) • PMIC: NXP PCA9451A
Physical	• Board size: SMARC 2.1 (Smart Mobility ARChitecture), 82 x 50 mm • Operating temperature: 0 to +70 °C (commercial), -40 to +85 °C (industrial) • Relative humidity: 10% to 90%

3.3 SoM Block Diagram



4. CPU Module Hardware Components

This chapter describes the hardware components of RNX-iMX93-SMARC SoM.

4.1 Power supply

RNX-iMX93-SMARC uses the NXP PCA9451A Power Management Integrated Circuit (PMIC), designed specifically for the i.MX 93 family of application processors. The PMIC generates all power rails required on the module from the single 5.0 V supply (VDD_IN).

The PMIC is programmable via I2C2 (I2C address 0x25) and interfaces directly with the processor through PMIC_ON_REQ, PMIC_STBY_REQ, POR_B, WDOG_B and an interrupt line (PMIC_nINT, read via the GPIO expander). A 32.768 kHz crystal on the PMIC provides the low-frequency clock (CLK_32K_OUT) for the i.MX 93 and the Wi-Fi module. Two additional regulators supply the Ethernet PHYs and the Wi-Fi module I/O.

Rail	Source	Voltage	Main loads
VDD_SOC	PCA9451A BUCK1 + BUCK3 (dual phase)	0.8 V	i.MX 93 core supply (VDD_SOC)
VDD_LPD4x_VDDQ	PCA9451A BUCK2	0.6 V	LPDDR4X VDDQ, i.MX 93 VDDQ_DDR
VDD_3V3	PCA9451A BUCK4	3.3 V	eMMC VCC, USB PHY 3.3 V, USB hub, Ethernet PHY AVDDH, Wi-Fi module, carrier pull-ups
VDD_1V8	PCA9451A BUCK5	1.8 V	i.MX 93 I/O and analog 1.8 V, LPDDR4X VDD1, eMMC VCCQ, Ethernet PHY DVDDH
NVCC_DRAM_1V1	PCA9451A BUCK6	1.1 V	LPDDR4X VDD2, i.MX 93 VDD2_DDR
NVCC_BBSM_1V8	PCA9451A LDO1	1.8 V	i.MX 93 battery-backed (BBSM) domain
VDD_ANA_0V8	PCA9451A LDO4	0.8 V	i.MX 93 analog, USB and MIPI 0.8 V supplies
NVCC_SD2_1V8_3V3	PCA9451A LDO5	1.8 / 3.3 V	SD card (SDIO) I/O voltage, selected by SD2_VSELECT
VDD_1V2	TPS62A01 buck (from VDD_3V3)	1.2 V	Ethernet PHY AVDDL / AVDDL_PLL
WIFI_1V8	NCP114 LDO (from VDD_3V3)	1.8 V	Wi-Fi module VIO (ensures the required 3.3 V before VIO sequencing)

4.2 CPU i.MX93

The i.MX 93 includes powerful dual Arm® Cortex®-A55 processors with speeds up to 1.7 GHz integrated with a NPU that accelerates machine learning inference. A general-purpose Arm® Cortex®-M33 running up to 250 MHz is for real-time and low-power processing. Robust control networks are possible via CAN-FD interface. Also, dual 1 Gbps Ethernet controllers, one supporting Time Sensitive Networking (TSN), drive gateway applications with low latency. The i.MX 93 industrial qualified part is particularly useful for applications such as:

• Industrial human machine interface (HMI)

• Industrial vision

• Scanning and printing

• EV Charging

• Industrial automation

• Touchless access control

• Energy meter

• Energy grid equipment

The module is equipped with the MIMX9352CVVXMAB (i.MX 9352, 14 x 14 mm FCBGA, industrial qualification). The design supports silicon revisions A1 and A2; the differences are handled by assembly options (see chapter 6.5).

4.2.1 CPU Block Diagram

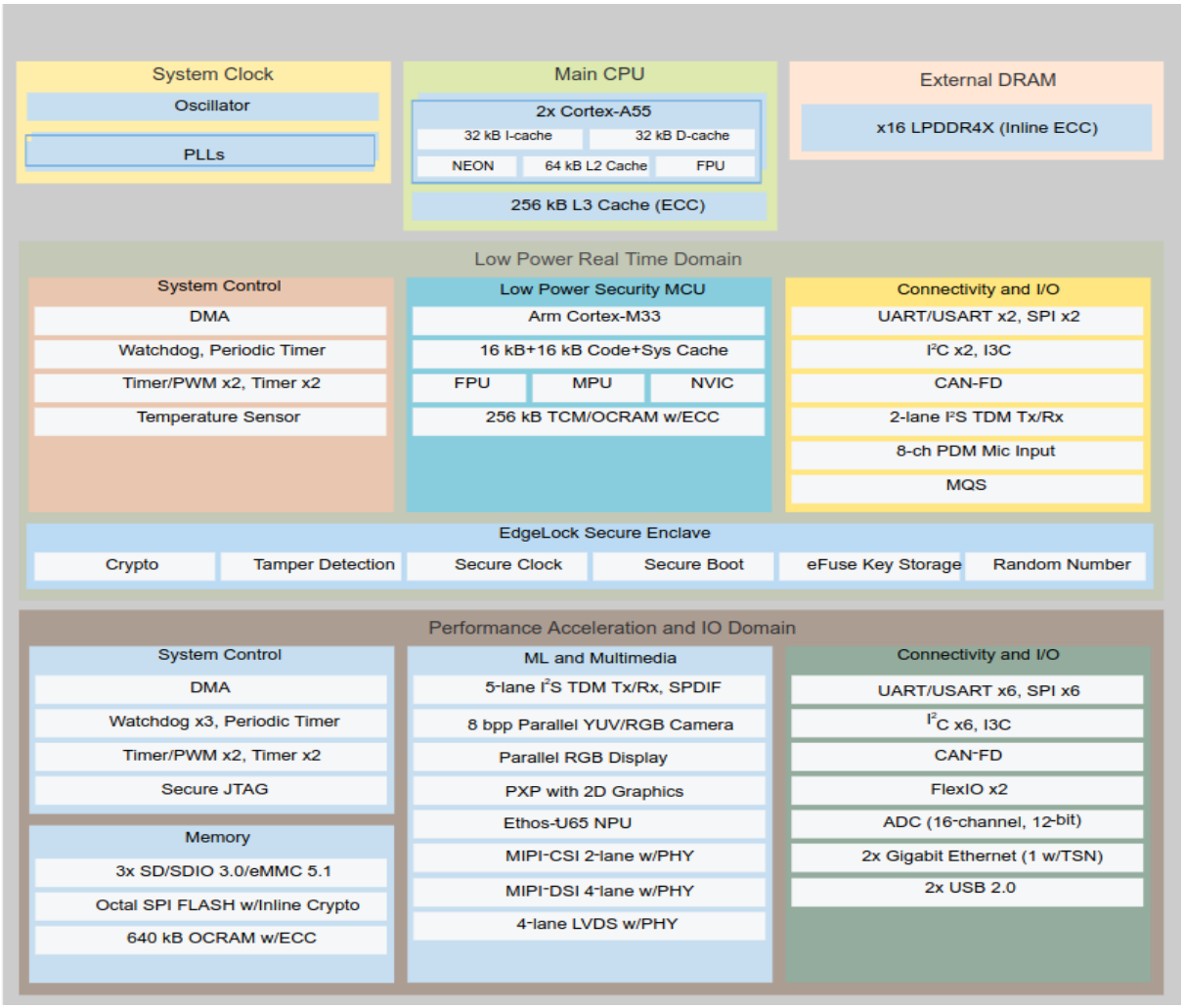


Figure 4.1: i.MX93 block diagram

4.2.2 CPU Platform

The i.MX93 processor implements two ARM® Cortex®-A55 cores intended for high level O/S, with an ARM® Cortex®-M33 core dedicated for real-time and security tasks.

The ARM Cortex-A55 platform has the following features:

- Dual ARM Cortex-A55 Cores
- Target frequency of 1.7GHz
- The core configuration is symmetric, where each core includes:

- 32 KByte L1 Instruction Cache
- 32 KByte L1 Data Cache
- 64 KByte L2 cache per core
- Media Processing Engine (MPE) with Arm® Neon™ technology supporting the Advanced SIMD architecture
- Floating Point Unit (FPU) supporting the Armv8.2-A floating-point architecture
- 256 KByte shared cluster L3 cache
- Core cache protection (parity/ECC) supported

The ARM Cortex-M33 platform includes the following features:

- Microcontroller available both for boot and for customer application
- Cortex-M33 CPU core operating at 250 MHz
- 16KB L1 Instruction Cache
- 16KB L1 Data Cache
- 256 KByte TCM, also accessible as SRAM by the rest of the system
- ECC support for both cache and TCM

4.3 Memory

4.3.1 DRAM

RNX-iMX93-SMARC is equipped as standard with 2 GiB LPDDR4X memory (IMAG16L4JCDG, single channel, dual rank). The data bus is 16-bit wide; the i.MX 93 DRAM controller supports data rates of up to 3733 MT/s and inline ECC. Other memory sizes are available on request.

4.3.2 eMMC – non-volatile storage memory

RNX-iMX93-SMARC is equipped as standard with 4 GB eMMC 5.1 (Samsung KLM4G1FETE), connected to uSDHC1 with an 8-bit bus (HS400 with data strobe). A 16 GB eMMC (ASFC16G31M) can be assembled optionally.

The eMMC can be used as boot device.

4.4 WLAN

The optional wireless interface is implemented with the AMPAK AP6275SDSR LGA module (Broadcom BCM43752 chipset). AP6275SDSR is an IEEE 802.11ax/ac/a/b/g/n Wi-Fi 6 + Bluetooth 5.0 combo module with two external antenna connectors.

Wi-Fi is connected to uSDHC3 (SDIO, 4-bit, 1.8 V). The Bluetooth PCM audio interface is connected to SAI1, which is shared with SMARC SPI1. The Bluetooth HCI UART can be connected to LPUART5 by assembly option (R63–R66, not populated by default); these pins are shared with the JTAG interface. WL_REG_ON, BT_REG_ON and the wake-up signals are controlled through the PCAL6416A GPIO expander. The 1.8 V I/O supply of the module (WIFI_1V8) is generated by a dedicated LDO from VDD_3V3, because the PMIC sequence (VDD_3V3 4–5 ms after VDD_1V8) does not meet the Wi-Fi module requirements. The 32.768 kHz sleep clock is provided by the PMIC.

Instead of AP6275SDSR, RNX-iMX93-SMARC can be assembled with the AzureWave AW-CM276NF module (IEEE 802.11ac/a/b/g/n + Bluetooth 5.0) on request.

4.5 USB Hub

An optional Microchip USB2514B 4-port USB 2.0 hub is connected to the i.MX 93 USB2 port (populated in the Full variant). Hub downstream ports 1–3 are routed to SMARC USB1, USB2 and USB3; port 4 is routed to SMARC USB4 or, by assembly option, to the USB interface of the Wi-Fi module. The hub runs from its own 24 MHz crystal, is held in reset by POR_B and its VBUS_DET input is controlled by the GPIO expander (P0_7).

4.6 GPIO Expander

An optional NXP PCAL6416A 16-bit I/O expander is connected to I2C2 (I2C address 0x20; 0x21 by assembly option). Port 1 provides six of the SMARC GPIOs, port 0 controls the Wi-Fi/Bluetooth module and the USB hub and reads the PMIC interrupt. The expander interrupt output is connected to CCM_CLKO2 (GPIO3_IO27); if the expander is not populated, R85 connects the PMIC interrupt directly to this pin. The expander is reset by POR_B.

Port	Signal	Function
P0_0	PMIC_nINT	PMIC interrupt (input)
P0_1	W_DISABLE1	Wi-Fi WL_GPIO1 / WL_DEV_WAKE
P0_2	W_DISABLE2	Bluetooth BT_REG_ON
P0_3	BT_UART_WAKEn	Bluetooth wake
P0_4	WL_HOST_WAKEn	Wi-Fi host wake (input)
P0_5	SDIO_RESETn	Wi-Fi WL_REG_ON

Port	Signal	Function
P0_6	HOST_WAKE_WLAN	Host-to-Wi-Fi wake
P0_7	USB_HUB_VBUS_DET	USB2514B upstream VBUS detect
P1_0 – P1_3	IOEXP_P1_0 – P1_3	SMARC GPIO8 – GPIO11
P1_4	IOEXP_P1_4	SMARC GPIO13
P1_5	IOEXP_P1_5	SMARC GPIO12
P1_6, P1_7	–	Not used

4.7 1-Wire

A DS2401P+ silicon serial number (or a DS2431P+ 1-Kbit 1-Wire EEPROM) can be populated optionally. GPIO2_IO28 is used for the 1-Wire interface. The same signal drives the green heartbeat LED DL1 and is available on the SMARC connector as GPIO7.

4.8 Boot Mode Selection

The i.MX 93 boot mode pins BOOT_MODE[3:0] are shared with UART1_TXD, UART2_TXD, SAI1_TXFS (SPI1_CS0#) and SAI1_TXD0 (SPI1_CK) and are sampled at power-on reset. They have internal pull-downs. The SMARC BOOT_SEL0#–BOOT_SEL2# inputs drive BOOT_MODE0–BOOT_MODE2 through PNP transistor buffers: a BOOT_SELx# pin connected to GND on the carrier sets the corresponding BOOT_MODEx to 1; an open BOOT_SELx# pin gives 0. BOOT_MODE3 is 0 (Cortex-A55 boot) unless the optional header J3 is populated and closed (Cortex-M33 boot).

BOOT_SEL2#	BOOT_SEL1#	BOOT_SEL0#	BOOT_MODE[2:0]	Boot device (Cortex-A55)
open	open	open	000	Boot from internal fuses
open	open	GND	001	Serial downloader (USB)
open	GND	open	010	On-module eMMC (uSDHC1, 8-bit)
open	GND	GND	011	Carrier SD card (uSDHC2, 4-bit)
GND	open	open	100	FlexSPI serial NOR – not supported on this module
GND	open	GND	101	FlexSPI serial NAND – not supported on this module
GND	GND	open	110	Infinite loop (debug)
GND	GND	GND	111	Test mode – do not use

Carrier circuits connected to SER1_TX, SER3_TX, SPI1_CS0# and SPI1_CK must not drive these signals during power-on reset, otherwise the boot mode may be changed.

5. SMARC 314-pin connector

The RNX-iMX93-SMARC is compliant with the SMARC 2.1.1 specification and uses the 314-pin MXM 3.0 edge connector. All signals are 1.8 V level unless stated otherwise. The following table lists the SMARC interfaces implemented on the module and their source (standard Full variant). Signals not listed are not connected.

The detailed pin-out of all 314 edge-connector pins – SMARC signal name, module net, i.MX 93 ball and pad, function used, SMARC and SoC I/O levels, all pad alternate functions (ALT0–ALT7), shared and multiplexed signals and assembly options – is provided in the Excel table RNX-iMX93-SMARC-Pinout.xlsx, available for download at:

https://download.ronetix.at/boards/doc/RNX-iMX93-SMARC/RNX-iMX93-SMARC-Pinout.xlsx

Partial schematics of the module are available at:

https://download.ronetix.at/boards/doc/RNX-iMX93-SMARC/RNX-iMX93-SMARC_Schematic_partial.PDF

SMARC signal	Module source / i.MX 93 signal	Notes
Power and management		
VDD_IN (P147–P156)	VSYS_5V	5.0 V ±5% module supply
POWER_BTN#	ONOFF	Power button input, internal pull-up
RESET_IN#	PMIC PMIC_RST_B (SYS_RST#)	Reset input, also on JTAG connector
CARRIER_PWR_ON	POR_B	High when module power is good
BOOT_SEL0# – BOOT_SEL2#	BOOT_MODE0 – BOOT_MODE2	See chapter 4.8
I2C_PM_CK / I2C_PM_DAT	LPI2C2 (I2C2_SCL / I2C2_SDA)	PMIC 0x25, GPIO expander 0x20
RESET_OUT#, VDD_RTC, WDT_TIME_OUT#, SLEEP#, LID#, BATLOW#, CARRIER_STBY#, FORCE_RECOV#, TEST#, SMB_ALERT#	–	Not connected
Gigabit Ethernet		
GBE0_MDI0± – MDI3±	ENET_QOS (ENET1 pads) + KSZ9131RNX	PHY address 1, TSN capable
GBE0_LINK100#, LINK1000#, LINK_ACT#	KSZ9131 LED outputs	Open drain
GBE1_MDI0± – MDI3±	ENET (ENET2 pads) + KSZ9131RNX	PHY address 2
GBE1_LINK100#, LINK1000#, LINK_ACT#	KSZ9131 LED outputs	Open drain
USB		
USB0±	i.MX 93 USB1	OTG
USB0_VBUS_DET	USB1_VBUS (divider)	5 V input

SMARC signal	Module source / i.MX 93 signal	Notes
USB0_OTG_ID	USB1_ID	3.3 V
USB0_EN_OC#	CCM_CLKO3 / GPIO4_IO28	3.3 V, open drain, 10 kΩ pull-up
USB1± – USB4±	USB2514B hub ports 1 – 4	Hub upstream = i.MX 93 USB2
USB1_EN_OC# – USB4_EN_OC#	10 kΩ pull-up to 3.3 V	USB1/USB3: GPIO4_IO29 by assembly option
USB3_VBUS_DET, USB3_OTG_ID	i.MX 93 USB2 VBUS / ID	Only in the variant without hub
SD card		
SDIO_CK, SDIO_CMD, SDIO_D0 – D3	uSDHC2	1.8 V / 3.3 V
SDIO_CD#	SD2_CD_B	
SDIO_PWR_EN	SD2_RESET_B	3.3 V
SDIO_WP	–	Not connected
Display and camera		
LVDS0_0± – 3±, LVDS0_CK± / DSI0_D0± – D3±, DSI0_CLK±	i.MX 93 LVDS or MIPI DSI	Assembly option, default LVDS
LCD0_VDD_EN	GPIO2_IO21	
LCD0_BKLT_EN	PDM_BIT_STREAM1 / GPIO1_IO10	
LCD0_BKLT_PWM	GPIO2_IO22 / TPM5_CH1	PWM
I2C_LCD_CK / I2C_LCD_DAT	LPI2C1	Shared with I2C_GP, I2C_CAM0
CSI0_CK±, CSI0_RX0±, CSI0_RX1±	i.MX 93 MIPI CSI	2 data lanes
CAM_MCK	CCM_CLKO1 / GPIO3_IO26	Camera master clock
I2C_CAM0_CK / I2C_CAM0_DAT	LPI2C1	Shared with I2C_GP, I2C_LCD
Serial interfaces		
SER0_TX/RX/RTS#/CTS#	LPUART5 (GPIO2_IO00 – IO03)	
SER1_TX/RX	LPUART1	Debug console; TX = BOOT_MODE0
SER2_TX/RX/RTS#/CTS#	LPUART6 (GPIO2_IO04 – IO07)	RTS# shared with SPI0_CS1#
SER3_TX/RX	LPUART2	TX = BOOT_MODE1
SPI0_CS0#, CS1#, CK, DIN, DO	LPSPI3 (GPIO2_IO07 – IO11)	CS1# shared with SER2_RTS#
SPI1_CS0#, CS1#, CK, DIN, DO	LPSPI1 (SAI1 pads, GPIO1_IO09)	Shared with Wi-Fi BT PCM; CS1# shared with CAN0_RX
I2C_GP_CK / I2C_GP_DAT	LPI2C1	2.2 kΩ pull-ups to 1.8 V
CAN0_TX / CAN0_RX	FlexCAN1 (GPIO1_IO08 / GPIO1_IO09)	CAN FD, transceiver on carrier
CAN1_TX / CAN1_RX	FlexCAN2 (GPIO2_IO25 / GPIO2_IO27)	CAN FD, transceiver on carrier
I2S0_CK, LRCK, SDOUT, SDIN, AUDIO_MCK	SAI3	See chapter 6.11

SMARC signal	Module source / i.MX 93 signal	Notes
GPIO		
GPIO0 – GPIO13	i.MX 93 GPIO2 / PCAL6416A	See chapter 6.10

6. CPU Module interfaces

6.1 Gigabit Ethernet

RNX-iMX93-SMARC implements two full-featured 10/100/1000 Mbps Ethernet ports using the MACs integrated in the i.MX 93 and two Microchip KSZ9131RNX RGMII Ethernet PHYs. SMARC GBE0 is connected to the ENET_QOS controller (ENET1 pads, PHY address 1) and GBE1 to the ENET controller (ENET2 pads, PHY address 2). Each PHY has its own MDIO bus and 25 MHz crystal; both PHYs share the reset signal GPIO2_IO29. The magnetics are placed on the carrier board.

- GBE1 (ENET): Energy Efficient Ethernet (EEE), Ethernet AVB and IEEE 1588
- GBE0 (ENET_QOS): Time Sensitive Networking (TSN) in addition to EEE, Ethernet AVB and IEEE 1588

Both interfaces support the following main features:

- 10/100/1000 BASE-T IEEE 802.3 compliant.
- IEEE 802.3u compliant Auto-Negotiation.
- IEEE 1588 time stamping in the MAC.
- Automatic channel swap (ACS).
- Automatic MDI/MDIX crossover.
- Automatic polarity correction.
- Activity and speed indicator LED controls.

6.2 Display interfaces

According to the SMARC specification, the LVDS and MIPI-DSI signals share same pins:

3.4.4 LVDS / eDP / MIPI DSI Pin Sharing

Pin #	LVDS Signal Name	MIPI DSI Signal Name
S125	LVDS0_0+	DSI0_D0+
S126	LVDS0_0-	DSI0_D0-
S128	LVDS0_1+	DSI0_D1+
S129	LVDS0_1 -	DSI0_D1-
S131	LVDS0_2+	DSI0_D2+
S132	LVDS0_2-	DSI0_D2-
S137	LVDS0_3+	DSI0_D3+
S138	LVDS0_3-	DSI0_D3-
S134	LVDS0_CK+	DSI0_CLK+
S135	LVDS0_CK-	DSI0_CLK-
S133	LCD0_VDD_EN	LCD0_VDD_EN
S127	LCD0_BKLT_EN	LCD0_BKLT_EN
S141	LCD0_BKLT_PWM	LCD0_BKLT_PWM
S144	-	DSI0_TE

Figure 6.1: SMARC LVDS, MIPI-DSI pin sharing

RNX-iMX93-SMARC can be assembled in two variants:

- LVDS (default): i.MX 93 LVDS signals on SMARC LVDS0 (S125–S138)
- MIPI DSI: i.MX 93 MIPI-DSI signals on SMARC DSI0 (S125–S138)

The selection is made with the 0 Ω resistors R161–R180. In both variants the display control signals LCD0_VDD_EN (GPIO2_IO21), LCD0_BKLT_EN (GPIO1_IO10), LCD0_BKLT_PWM (GPIO2_IO22, TPM5_CH1) and the I2C_LCD bus (LPI2C1) are available. DSI0_TE is not connected.

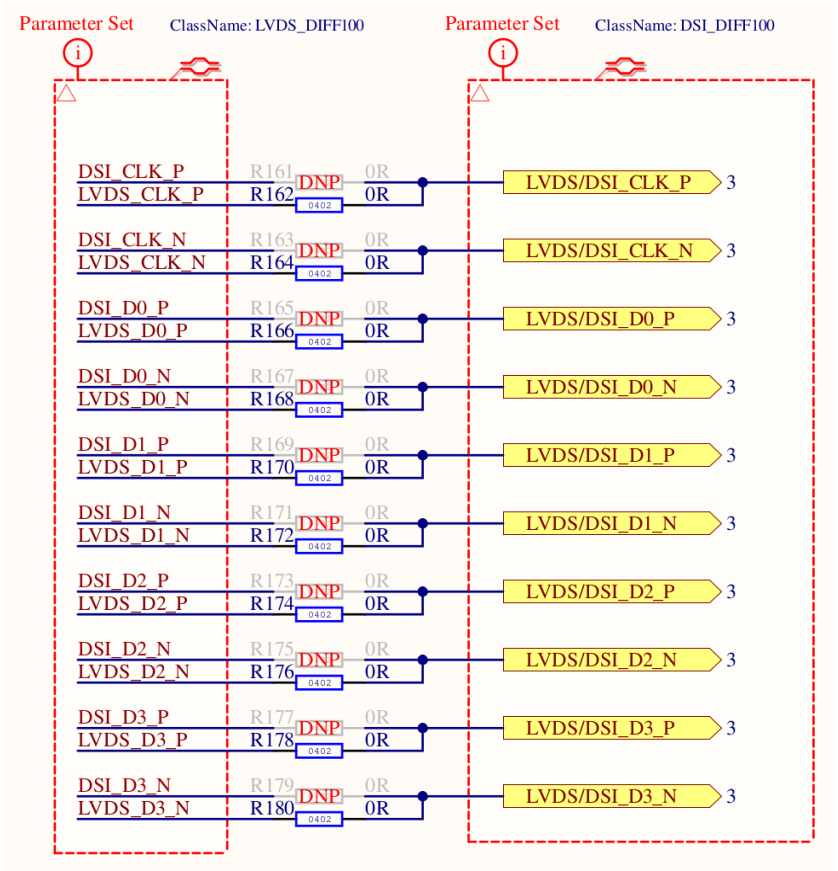


Figure 6.2: LVDS/MIPI-DSI pin sharing

- MIPI DSI

  The MIPI-DSI interface is based on the four-lane MIPI display interface of the i.MX 93.

  The i.MX 93 supports one 4-lane MIPI DSI display with pixels from the LCDIF. The key features of the MIPI DSI (controller and PHY) include:

  - Conforms to MIPI-DSI specification v1.2 and MIPI-DPHY specification v1.2
  - Maximum resolution limited by a 200 MHz pixel clock and an active pixel rate of 140 Mpixel/s with 24-bit RGB; this includes resolutions such as 1080p60 or 1920x1200p60
  - Support up to 4 Tx data lanes (plus 1 Tx clock lane)
  - Support 80Mbps - 1.5Gbps data rate per lane in high speed operation
  - Support 10Mbps data rate in low power operation

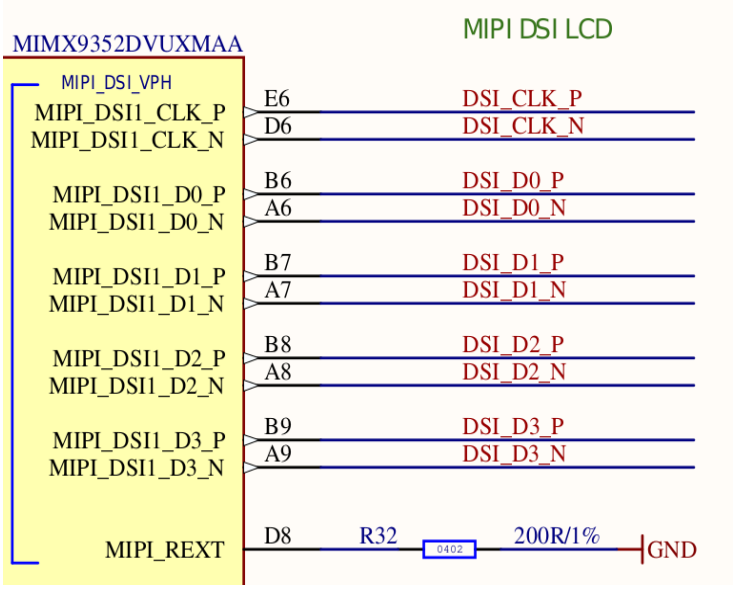


Figure 6.3: MIPI-DSI

- LVDS

  The LVDS interface is based on the four-lane LVDS display interface of the i.MX 93.

  The LVDS Display Bridge (LDB) connects to an External LVDS Display Interface. The purpose of the LDB is to support flow of synchronous RGB data to external display devices through the LVDS interface.

  - Supports FPD-Link
  - Supports single channel (4 lanes) output at up to 80MHz pixel clock and LVDS clock, with 7:1 ratio from LVDS data to pixel clock, implying up to 560Mbps LVDS data rate. This supports resolutions up to approximately 1366x768p60 or 1280x800p60.
  - Supports VESA and JEIDA pixel mapping
  - Supports an LVDS transmitter with four 7-bit channels. Each channel sends 6 pixel bits and one control signal at 7 times the pixel clock rate.

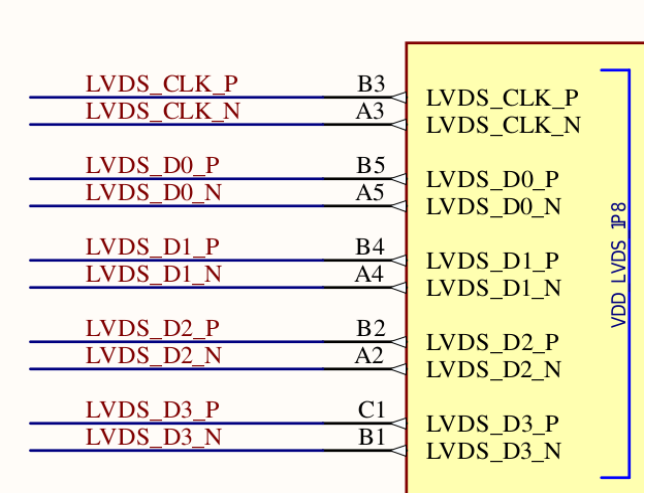


Figure 6.4: LVDS Interface

6.3 MIPI-CSI Camera interface

The MIPI-CSI interface is based on the two-lane MIPI CSI-2 camera interface of the i.MX 93. The clock lane and two data lanes are available on SMARC CSI0 (CSI0_CK±, CSI0_RX0±, CSI0_RX1±). The camera master clock CAM_MCK is generated by CCM_CLKO1, the camera control bus I2C_CAM0 is LPI2C1, and SMARC GPIO0–GPIO3 can be used as CAM0/CAM1 power-down and reset signals. CSI1 is not supported.

The MIPI Rx D-PHY includes the following features:

- Compliant to MIPI D-PHY interface specification, revision 1.2
- Lane operation ranging from 80 Mbps to 1.5 Gbps in forward direction
- Aggregate throughput up to 3 Gbps with two data lanes
- Maximum LP data rate supported of 10 Mbps
- PHY-Protocol Interface (PPI) for clock and data lanes
- Low-power Escape modes and Ultra Low Power state
- HS RX Equalizer up to 3dB
- Optional usage of external reference resistor (200 ohm)
- HS RX automatic offset cancellation

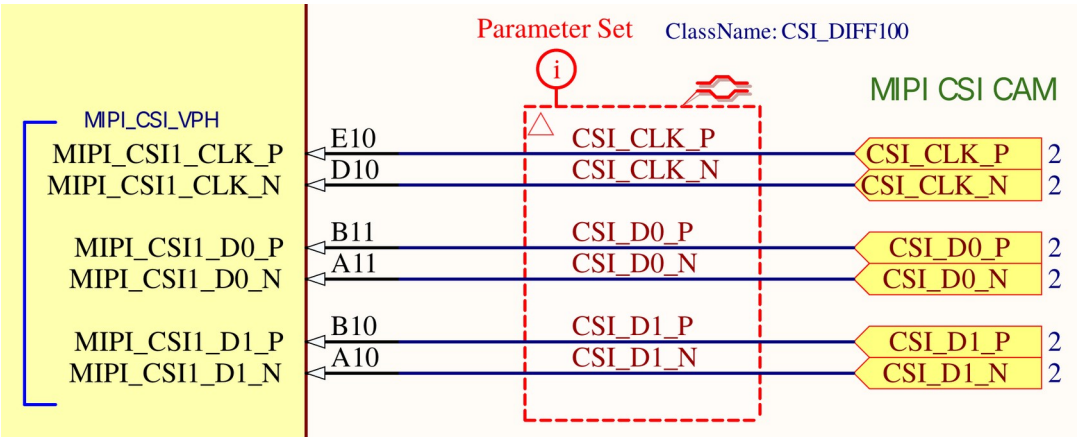


Figure 6.5: MIPI-CSI

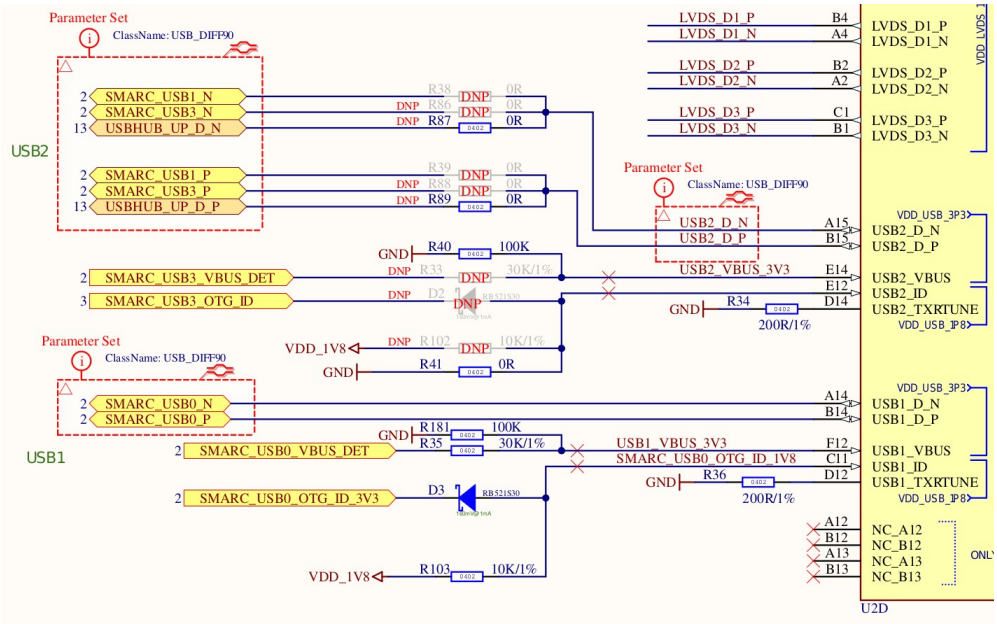
6.4 USB interface

The i.MX93 SoC is equipped with two USB OTG controllers and PHYs. Each USB instance contains a USB 2.0 core. Both ports support dual-role functionality.

On RNX-iMX93-SMARC the i.MX 93 USB1 port is connected to SMARC USB0 (OTG, with USB0_VBUS_DET, USB0_OTG_ID and USB0_EN_OC#). Depending on the assembly variant, the i.MX 93 USB2 port is connected to the on-module USB2514B hub (Full variant: hub ports 1–4 drive SMARC USB1–USB4, port 4 alternatively the Wi-Fi module), directly to SMARC USB1 (host mode), or to SMARC USB3 (OTG mode, with USB3_VBUS_DET and USB3_OTG_ID). SMARC USB0_EN_OC# is controlled by GPIO4_IO28 through an open-drain level shifter; the other USBx_EN_OC# signals have 10 kΩ pull-ups to 3.3 V.

The USB ports support the following main features:

- High-Speed/Full-Speed/Low-Speed OTG core
- Hardware support for OTG signaling, session request protocol, and host negotiation protocol
- up to 8 endpoints
- Low-power mode with local and remote wake-up capability



- *Figure 6.6: USB*

6.5 MMC, SD, SDIO

The i.MX 93 is equipped with three uSDHC controllers. uSDHC1 is connected to the on-module eMMC (8-bit). uSDHC2 is available on the SMARC SDIO interface (4-bit); its I/O voltage is switched between 3.3 V and 1.8 V by the PMIC LDO5 under control of SD2_VSELECT, so UHS-I cards are supported. SDIO_PWR_EN is driven by SD2_RESET_B through a 3.3 V level shifter. uSDHC3 is connected to the Wi-Fi module.

Note: on i.MX 93 silicon revision A1, the NVCC_SD2, NVCC_WAKEUP and NVCC_AON supply groups must not be operated at 3.3 V. On modules with A1 silicon the SD2 signals therefore pass through an NXS0506 voltage-level translator (U12) and NVCC_SD2 is supplied with 1.8 V. On A2 silicon the translator is replaced by 0 Ω resistors (R202–R207) and NVCC_SD2 is supplied directly from LDO5.

The uSDHC supports the following main features:

- Conforms to the SD Host Controller Standard Specification version 2.0/3.0
- Compatible with the eMMC System Specification version 4.2/4.3/4.4/4.41/4.5/5.0/5.1
- Compatible with the SD Memory Card Specification version 3.0 and supports the Extended Capacity SD Memory Card

- Card bus clock frequency up to 200 MHz (eMMC HS400, SD SDR104)
- Supports 1-bit/4-bit SD and SDIO modes, and 1-bit/4-bit/8-bit eMMC modes
- Supports single block/multi-block read and write
- Supports block sizes of 1 ~ 4096 bytes
- Embodies two fully configurable 256x32-bit FIFO for read/write data

6.6 UART

The RNX-iMX93-SMARC exposes four UART interfaces, all based on the i.MX 93 LPUART controllers:

SMARC	i.MX 93	Signals	Notes
SER0	LPUART5	TX, RX, RTS#, CTS# (GPIO2_IO00 – IO03)	
SER1	LPUART1	TX, RX	Linux debug console; TX is BOOT_MODE0
SER2	LPUART6	TX, RX, RTS#, CTS# (GPIO2_IO04 – IO07)	RTS# shared with SPI0_CS1#
SER3	LPUART2	TX, RX	TX is BOOT_MODE1

All RX and CTS# inputs have 100 kΩ pull-ups to 1.8 V on the module. The i.MX 93 LPUART supports the following features:

- Full-duplex operation, standard NRZ format
- Programmable baud rate with configurable oversampling
- 7-, 8-, 9- or 10-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none)
- Transmit and receive FIFOs with DMA support
- Hardware flow control (RTS/CTS) and RS-485 transmitter enable output
- IrDA 1.0 compatible infrared mode
- LIN break detection and generation
- Idle-line and address-match detection (multidrop / 9-bit mode)
- Wake-up from low-power modes

6.7 I2C

The i.MX 93 is equipped with eight LPI2C controllers; two of them are used on the module. All I2C buses are 1.8 V with 2.2 kΩ pull-ups on the module.

LPI2C1 is available on the SMARC connector on the following pins:

- S5 / S7 – I2C_CAM0_CK / I2C_CAM0_DAT
- S48 / S49 – I2C_GP_CK / I2C_GP_DAT
- S139 / S140 – I2C_LCD_CK / I2C_LCD_DAT

LPI2C2 connects the on-module PMIC (address 0x25) and GPIO expander (address 0x20) and is available on the SMARC connector on pins P121 / P122 – I2C_PM_CK / I2C_PM_DAT.

The following general features are supported by all I2C bus interfaces:

- Compliant with the NXP I2C-bus specification (UM10204)
- Standard-mode (100 kbit/s), Fast-mode (400 kbit/s) and Fast-mode Plus (1 Mbit/s); high-speed and ultra-fast modes supported by the controller
- Multi-master operation
- Master or slave operation, SMBus support

I2C usage table:

I2C USAGE AND ADDRESS TABLE

NAME	PERIPHERAL	ADDRESS
I2C1 1.8V		
I2C2 1.8V	PMIC control	(0x25<<1)+RW
	GPIO Expander, PCAL6416AHF	(0x20<<1)+RW

Figure 6.7: I2C address usage

6.8 SPI

Two SPI interfaces are available on the SMARC connector, both derived from the i.MX 93 Low-Power SPI (LPSPI) controllers. SMARC SPI0 is connected to LPSPI3 (SPI0_CS1# is shared with SER2_RTS#). SMARC SPI1 is connected to LPSPI1 on the SAI1 pads (SPI1_CS1# is shared with CAN0_RX). SPI1 is not available when the Wi-Fi/Bluetooth module uses SAI1 for PCM audio

(R70–R74), and SPI1_CS0# / SPI1_CK are boot mode pins (see chapter 4.8). The following features are supported:

- Master or slave operation
- Full-duplex synchronous serial interface
- Two chip selects per SMARC SPI port (up to four per LPSPI controller)
- Configurable clock polarity and phase
- Command, transmit and receive FIFOs
- Continuous transfer mode for unlimited transfer length
- Direct Memory Access (DMA) support

6.9 CAN signals

The i.MX 93 FlexCAN controllers implement the CAN FD protocol according to ISO 11898-1:2015 and the CAN 2.0 B protocol specification.

RNX-iMX93-SMARC provides two CAN interfaces on the SMARC connector: CAN0 is connected to FlexCAN1 (CAN0_RX is shared with SPI1_CS1#) and CAN1 to FlexCAN2. The CAN transceivers must be placed on the carrier board.

6.10 GPIO

On the carrier board interface 14 GPIOs are available: 8 of them are provided directly by the i.MX 93 (1.8 V), the remaining 6 by the PCAL6416A I2C GPIO expander (1.8 V).

SMARC signal	Source	Alternate function / note
GPIO0 / CAM0_PWR#	GPIO2_IO12	
GPIO1 / CAM1_PWR#	GPIO2_IO13	
GPIO2 / CAM0_RST#	GPIO2_IO14	
GPIO3 / CAM1_RST#	GPIO2_IO15	
GPIO4 / HDA_RST#	GPIO2_IO18	
GPIO5 / PWM_OUT	GPIO2_IO23	TPM6_CH1 (PWM)
GPIO6 / TACHIN	GPIO2_IO24	TPM3_CH3 (capture)
GPIO7	GPIO2_IO28	Also heartbeat LED and optional 1-Wire
GPIO8 – GPIO11	PCAL6416A P1_0 – P1_3	
GPIO12	PCAL6416A P1_5	
GPIO13	PCAL6416A P1_4	

6.11 I2S Audio

One I2S interface is available on the SMARC connector. It is connected to the i.MX 93 SAI3 controller, which supports I2S, left-justified, TDM and AC97 formats. The audio codec is placed on the carrier board; it can be controlled through I2C_GP.

SMARC signal	i.MX 93 signal	Pad
I2S0_CK	SAI3_TX_BCLK	GPIO2_IO16
I2S0_LRCK	SAI3_TX_SYNC	GPIO2_IO26
I2S0_SDOUT	SAI3_TXD0	GPIO2_IO19
I2S0_SDIN	SAI3_RXD0	GPIO2_IO20
AUDIO_MCK	SAI3_MCLK	GPIO2_IO17

6.12 JTAG

The i.MX 93 debug access port (Arm® CoreSight™ DAP) supports JTAG (IEEE 1149.1) and Arm Serial Wire Debug (SWD). The signals are available on J2, a 10-pin 1.0 mm pitch JST SH connector (SM10B-SRSS-TB), with 1.8 V signal levels. The JTAG pins are shared with LPUART5, which can optionally be used as Bluetooth HCI UART.

J2 pin	Signal	Description
1	VDD_1V8	Reference voltage for the debugger (1.8 V)
2	–	Not connected
3	JTAG_TMS / SWDIO	Test mode select / SWD data
4	JTAG_TDO / SWO	Test data out / trace output
5	JTAG_TDI	Test data in
6	JTAG_TCK / SWCLK	Test clock / SWD clock
7	–	Not connected
8	SYS_RST#	System reset (PMIC reset input)
9	–	Not connected
10, M1, M2	GND	Ground

7. Power Supply

7.1 Power supply from base board

RNX-iMX93-SMARC is powered from a single regulated 5.0 V supply through the SMARC VDD_IN pins (P147–P156). Note that the module requires 5.0 V ±5%; the wider VDD_IN range of

3.0 V to 5.25 V allowed by the SMARC specification is not supported. VDD_RTC (S147) is not used; the i.MX 93 real-time clock is not battery-backed.

Signal	Type	Description
VDD_IN	Power input	Main power supply 5.0 V (P147–P156)
GND	Power input	Common ground

7.2 System Signals

Signal	Type	Description
POWER_BTN# (P128)	Input, pull-up	Connected to the i.MX 93 ONOFF input (debounced). A short connection to GND in the OFF state turns the module on. In the ON state a short connection to GND generates an interrupt (intended for software-controlled power down); holding it low for more than ~5 s forces the module off.
RESET_IN# (P127)	Input, pull-up	Connected to the PMIC reset input PMIC_RST_B (net SYS_RST#). A low level resets the module. Also available on the JTAG connector.
CARRIER_PWR_ON (S154)	Output	Connected to POR_B. High when the module power rails are valid and the processor is out of reset; can be used to enable the carrier power supplies.
BOOT_SEL0# – BOOT_SEL2# (P123 – P125)	Input	Boot device selection, see chapter 4.8. Leave open or connect to GND.
RESET_OUT# (P126)	–	Not connected

8. Electrical Specifications

8.1 Absolute maximum ratings

Parameter	Min	Max	Unit
VDD_IN – Main power supply	-0.5	5.5	V

8.2 Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
VDD_IN – Main power supply	4.75	5.0	5.25	V

Parameter	Min	Typ	Max	Unit
VDD_IN – recommended source capability		4.0		A

9. Operating Temperature Ranges

Range	Temp.
Commercial	0° to +70°C
Industrial	-40° to +85°C

10. Warranty Terms

Ronetix guarantees hardware products against defects in workmanship and material for a period of one (1) year from the date of shipment. Your sole remedy and Ronetix's sole liability shall be for Ronetix, at its sole discretion, to either repair or replace the defective hardware product at no charge or to refund the purchase price. Shipment costs in both directions are the responsibility of the customer. This warranty is void if the hardware product has been altered or damaged by accident, misuse or abuse.

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