COVER PAGE

RNX-iMX93-SMARC v1.2
Variant: A1-Full-AP6275SDSR_b11
Complies with SMARC v2.1.1

04/11/2026

GIT Revision:

9f729d61f0c959b8c6888bb1ba33528eea4bb3ce [Locally Modified]

Release notes v1.2:
- in PCB: no parts moved; v1.1 stencil remains compatible.
- fixed bug in PCB: connect R3 to VDD_1V8
- fixed bug in PCB: connect C66 to VDD_1V8
- fixed bug in PCB: connect R32 to CPU ball D8
- change R7 from 100K to 10K
- R202-R207 - are DNP if U12 is populated (CPU rev A1)

Release Notes v1.1:
Add 240R/1% to LPDDR4 ZQ1 (R110 to ball A8)
Chnaged LPDDR4 to IMAG16L4JCDG-046I (2 GB)
Add DL1 - heartbeat
Add various test points
Changed FB2,FB3,FB5,FB6 from BLM15AG221SN1D to BLM18PG121SN1D
Changed FB4, FB7 from MMZ1005Y152CT000 to BLM15AG221SN1D
Add voltage level shifter to all SD2 signals because in i.MX93 rev A1 the following groups can't be connected to 3.3V: NVCC_SD2, NVCC_WAKEUP, NVCC_AON. In CPU rev A2 is this bug is fixed and the voltage level shifter can be bypassed.

I2C USAGE AND ADDRESS TABLE

NAME	PERIPHERAL	ADDRESS
I2C1		
1.8V		
I2C2	*PMIC control*	*(0x25<<1)+RW*
1.8V	*GPIO Expander, PCAL6416AHF*	*(0x20<<1)+RW*

PCB1

PCB

FR4, ENIG, 1.2mm THICKNESS, GREEN SOLDER MASK

PCB_RNX-iMX93-SMARC v1.2

Multiplexing:
SMARC SPI1 is not available when SAI1 used in Wi-Fi
SMARC SPI1_CS1 is not available when CAN1_RX is used
SMARC SPI1_CS0 is not available when SER2_RTS is used

Assembling variants:
i.MX93 USB2 port can be connected to SMARC USB1 (HOST mode) or SMARC USB3 (OTG mode)

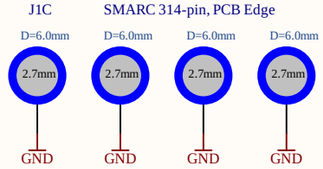
DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes.

DESIGN NOTE:
Example text for critical design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

J1C SMARC 314-pin, PCB Edge



Fiducials

FIDICIALS 3x TOP FIDICIALS 3x BOTTOM

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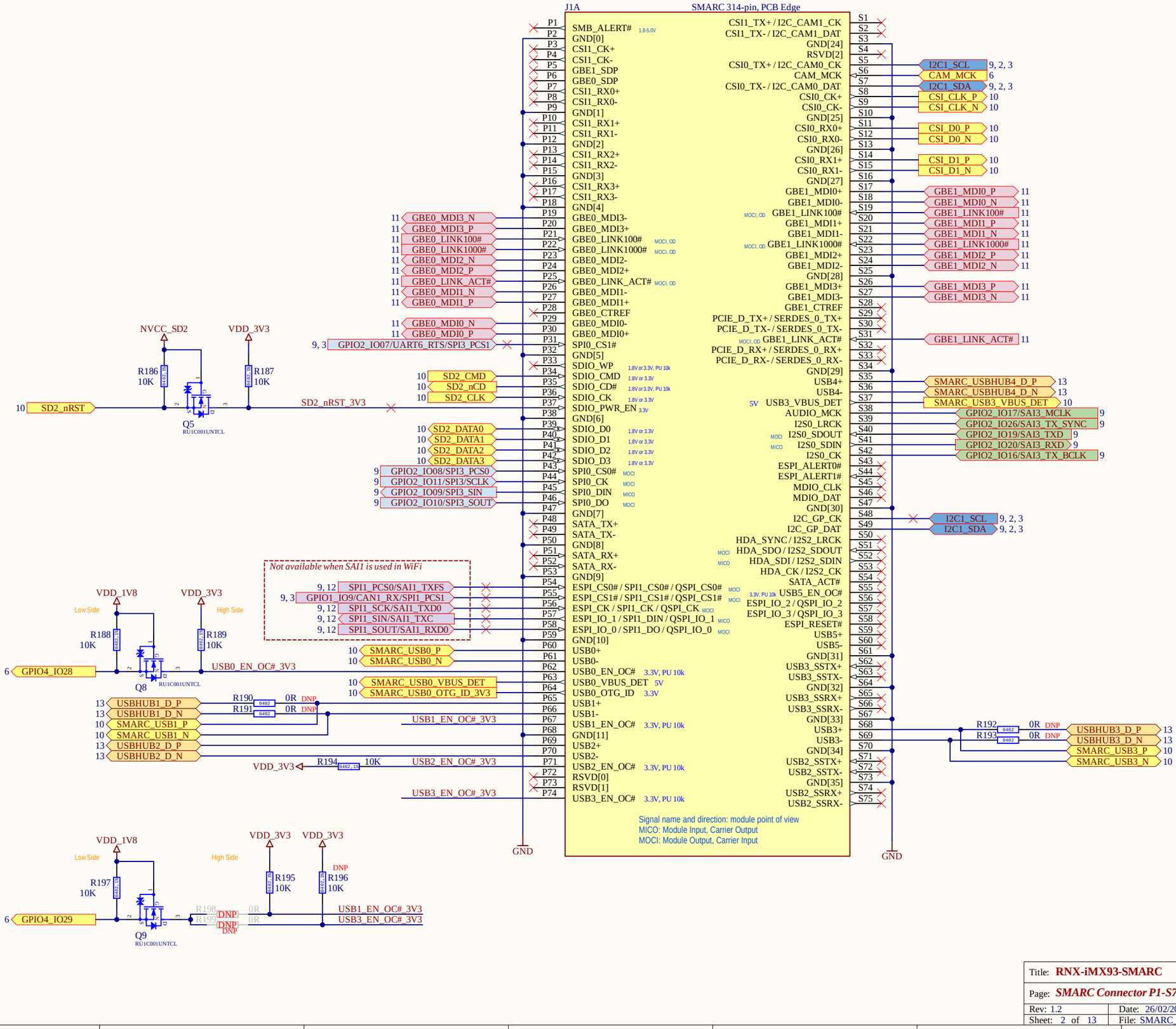
RONETIX DEVELOPMENT TOOLS

SMARC Connector P1-S75



Title:	**RNX-iMX93-SMARC**
Page:	***SMARC Connector P1-S75***
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Ronetix GmbH
Seeadlerweg 29
1220 Vienna
Austria

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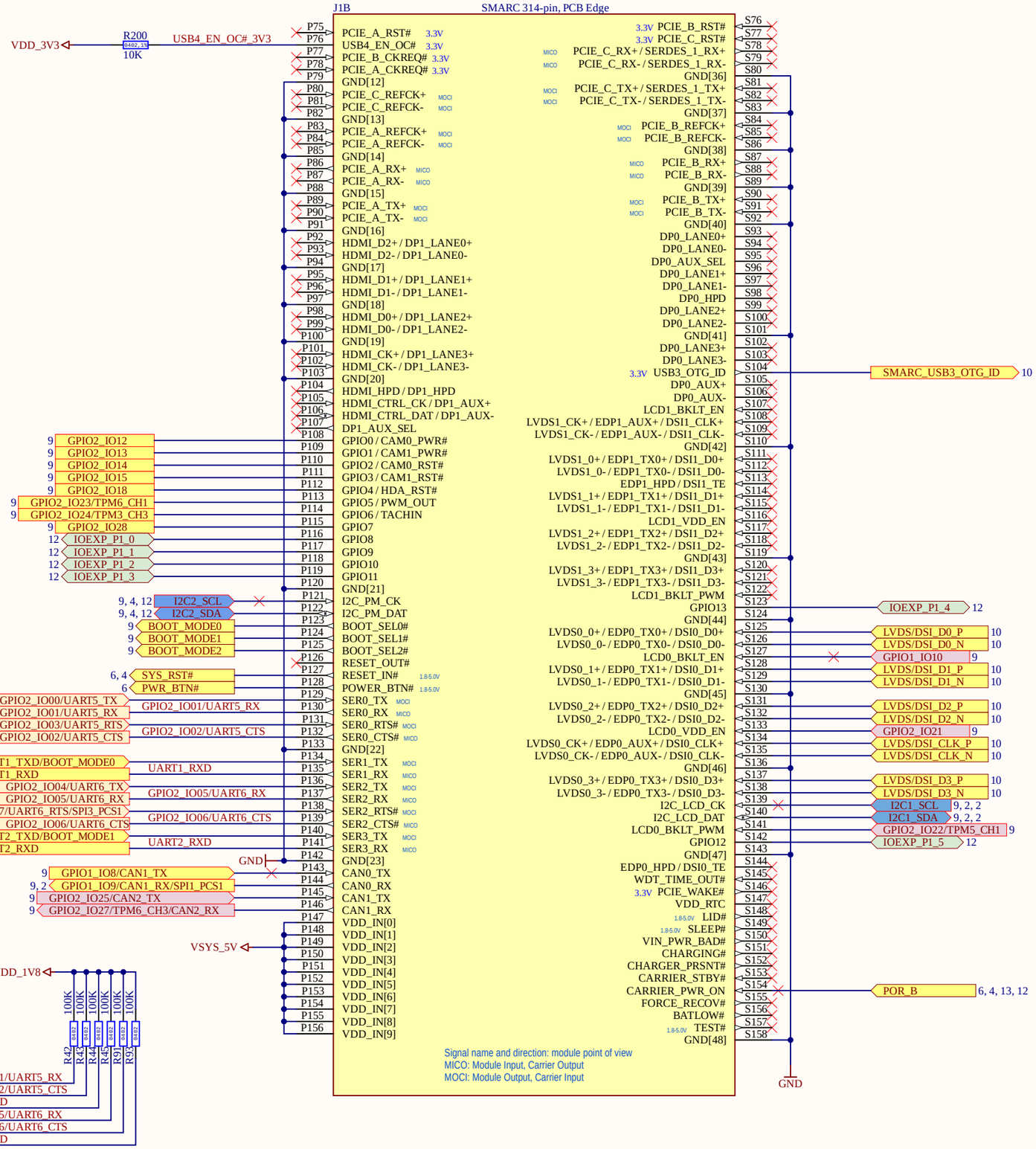
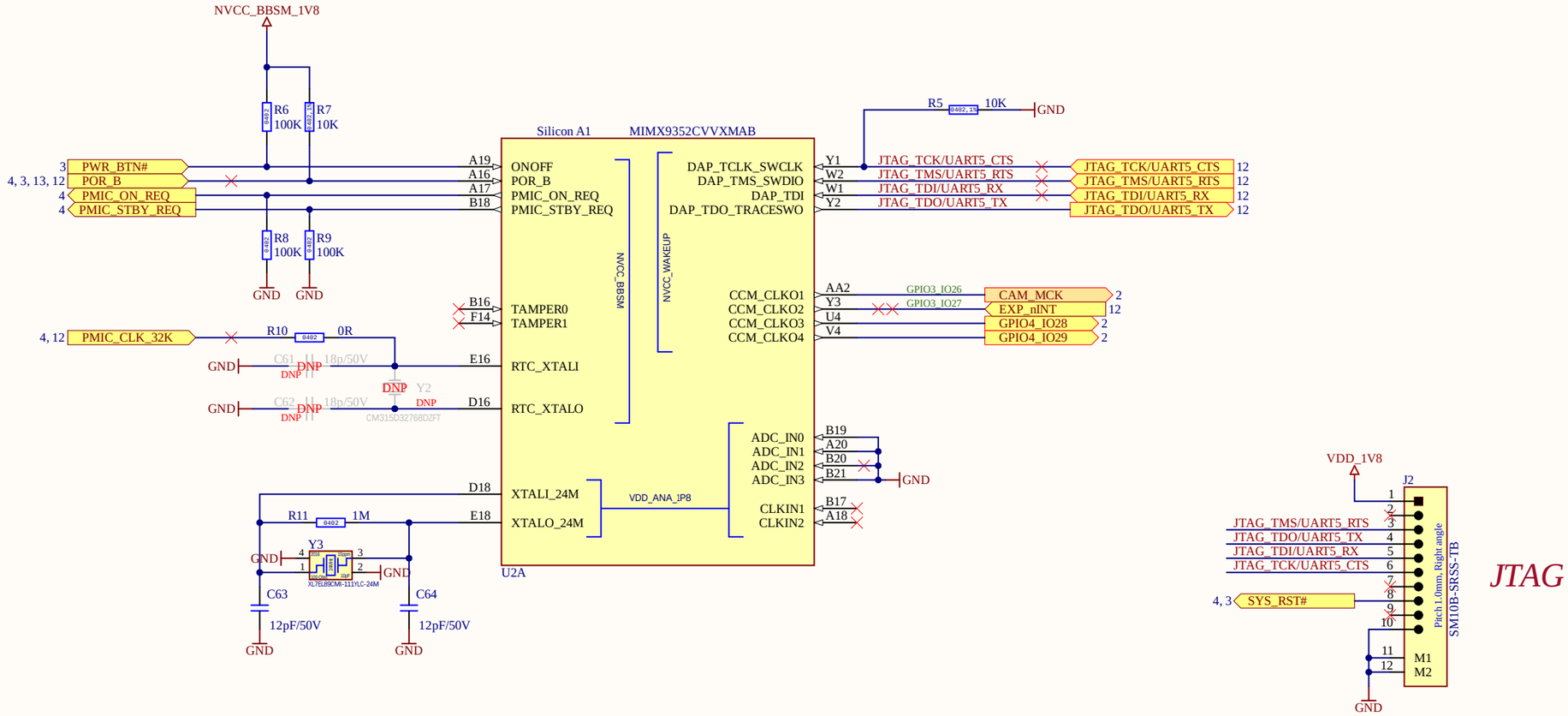
SMAC Connector P75-S158



Title: **RNX-iMX93-SMARC**			*Ronetix GmbH*
Page: ***SMAC Connector P75-S158***			*Seeadlerweg 29*
Rev: 1.2	Date: 14/02/2025	Size: A3	*1220 Vienna*
Sheet: 3 of 13	File: SMARC_conn-2.SchDoc		*Austria*

RONETIX DEVELOPMENT TOOLS

CPU Control



Title: **RNX-iMX93-SMARC**			*Ronetix GmbH*
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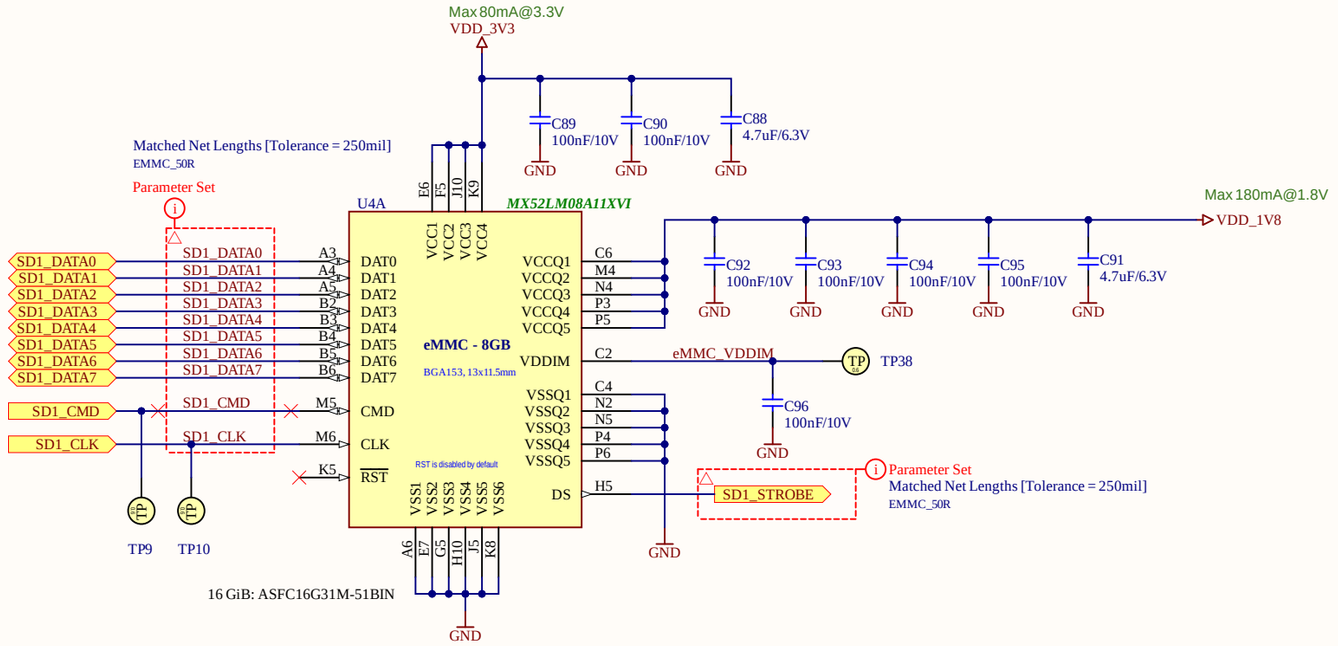
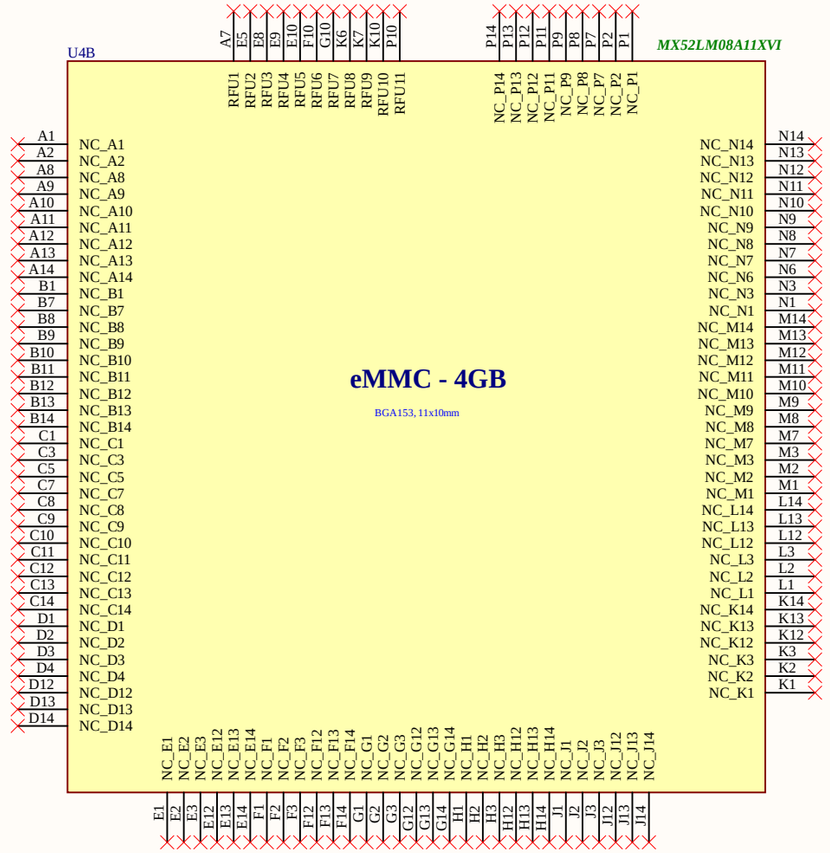
RONETIX DEVELOPMENT TOOLS

eMMC





Title: **RNX-iMX93-SMARC**			*Ronetix GmbH*
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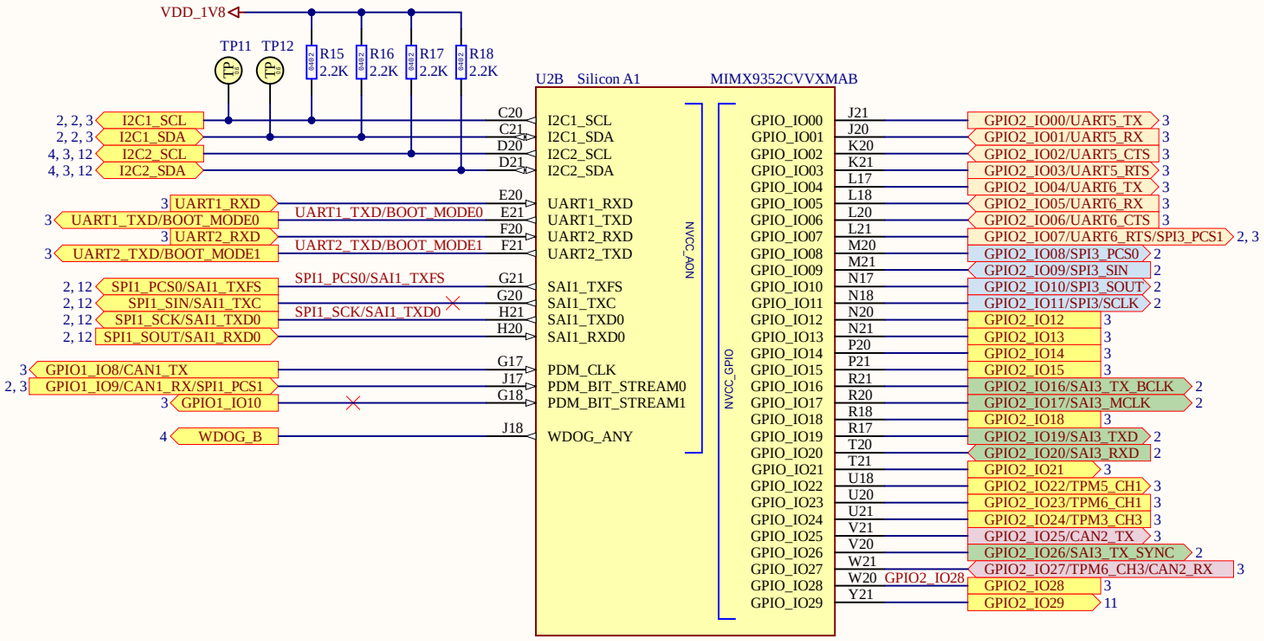
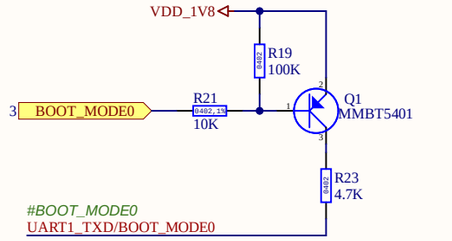
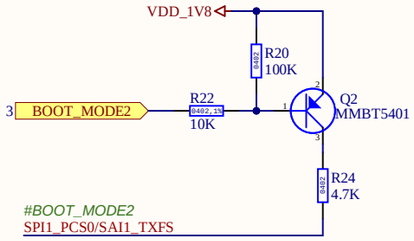
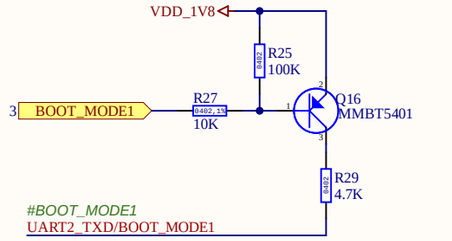
RONETIX DEVELOPMENT TOOLS

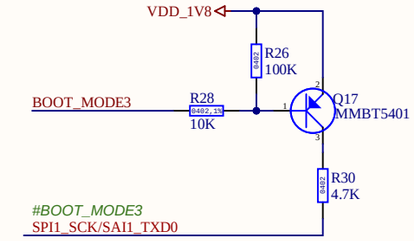
CPU - GPIO & BOOT

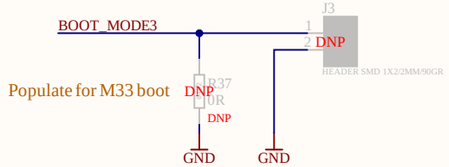






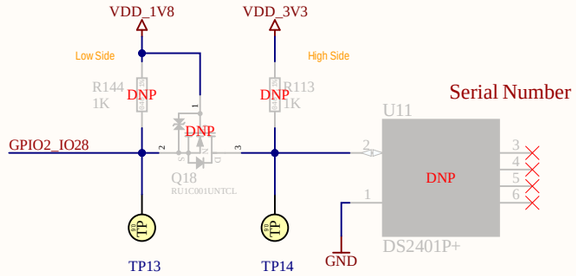


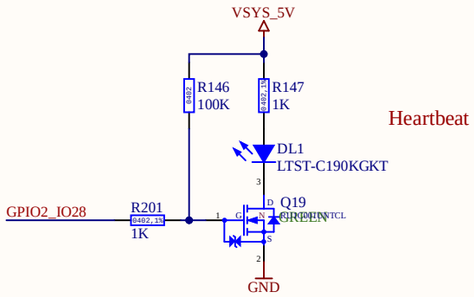




CPU pins: #BOOT_MODE[3:0]	BOOT CORE	BOOT DEVICE	COMMENT
0000	Cortex-A55	From internal fuses	
0001	Cortex-A55	Serial Downloader	USB1/2
0010	Cortex-A55	USDHC1 8-bit eMMC 5.1	with SFDP (JESD-216) discoverable
0011	Cortex-A55	USDHC2 4-bit SD3.0	parameters
0100	Cortex-A55	FlexSPI Serial NOR	
0101	Cortex-A55	FlexSPI Serial NAND 2K page	
0110	Cortex-A55	Infinite Loop	
0111	Cortex-A55	Test Mode	
1000	Cortex-M33	From internal fuses	
1001	Cortex-M33	Serial Downloader	USB1
1010	Cortex-M33	USDHC1 8-bit eMMC 5.1	with SFDP (JESD-216) discoverable
1011	Cortex-M33	USDHC2 4-bit SD3.0	parameters
1100	Cortex-M33	FlexSPI Serial NOR	
1101	Cortex-M33	FlexSPI Serial NAND 2K page	
1110	Cortex-M33	Infinite Loop	
1111	Cortex-M33	Test Mode	

SoC boot mode pins are inputs with pull-downs.
Pull-down:
27k-32k-38k <MIN-TYP-MAX>





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CPU - PHY

In CPU rev A1 populate U12 and not populate R202-R207
In CPU rev A2 do not populate U12 and populate R202-R207

eMMC

SD2_CLK	R207	DNP	0R	DNP	SD2_CLK_R
SD2_CMD	R202	DNP	0R	DNP	SD2_CMD_R
SD2_DATA0	R203	DNP	0R	DNP	SD2_DATA0_R
SD2_DATA1	R204	DNP	0R	DNP	SD2_DATA1_R
SD2_DATA2	R205	DNP	0R	DNP	SD2_DATA2_R
SD2_DATA3	R206	DNP	0R	DNP	SD2_DATA3_R

WiFi

MicroSD

NVCC_SD2_1V8_3V3 VDD_1V8

U12 NXS0506GU

VCCB 1.7-3.6V <= VCCA 1.1-1.95V
104Mbps 16-XQFN

C151 100nF/10V C152 100nF/10V

Silicon A1 MIMX9352CVVXMAB

U2C

NVCC_WAKEUP NVCC_SD2

Parameter Set ClassName: ENET1_RGMGII_TX_50R
Matched Net Lengths [Tolerance = 250mil]
Length Constraint [Min Length = 0mil Max Length = 1750mil]
ENET1_TD0 ENET1_TD1 ENET1_TD2 ENET1_TD3 ENET1_TXC ENET1_TX_CTL

Parameter Set ClassName: ENET1_RGMGII_RX_50R
Matched Net Lengths [Tolerance = 250mil]
Length Constraint [Min Length = 0mil Max Length = 1750mil]
ENET1_RD0 ENET1_RD1 ENET1_RD2 ENET1_RD3 ENET1_RXC ENET1_RX_CTL

Parameter Set ClassName: ENET2_RGMGII_TX_50R
Matched Net Lengths [Tolerance = 250mil]
Length Constraint [Min Length = 0mil Max Length = 1750mil]
ENET2_TD0 ENET2_TD1 ENET2_TD2 ENET2_TD3 ENET2_TXC ENET2_TX_CTL

Parameter Set ClassName: ENET2_RGMGII_RX_50R
Matched Net Lengths [Tolerance = 250mil]
Length Constraint [Min Length = 0mil Max Length = 1750mil]
ENET2_RD0 ENET2_RD1 ENET2_RD2 ENET2_RD3 ENET2_RXC ENET2_RX_CTL

Parameter Set ClassName: LVDS_DIFF100
Parameter Set ClassName: DSI_DIFF100

DSI_CLK_P	R161	DNP	0R	LVDS/DSI_CLK_P	3
LVDS_CLK_P	R162	DNP	0R		
DSI_CLK_N	R163	DNP	0R	LVDS/DSI_CLK_N	3
LVDS_CLK_N	R164	DNP	0R		
DSI_D0_P	R165	DNP	0R	LVDS/DSI_D0_P	3
LVDS_D0_P	R166	DNP	0R		
DSI_D0_N	R167	DNP	0R	LVDS/DSI_D0_N	3
LVDS_D0_N	R168	DNP	0R		
DSI_D1_P	R169	DNP	0R	LVDS/DSI_D1_P	3
LVDS_D1_P	R170	DNP	0R		
DSI_D1_N	R171	DNP	0R	LVDS/DSI_D1_N	3
LVDS_D1_N	R172	DNP	0R		
DSI_D2_P	R173	DNP	0R	LVDS/DSI_D2_P	3
LVDS_D2_P	R174	DNP	0R		
DSI_D2_N	R175	DNP	0R	LVDS/DSI_D2_N	3
LVDS_D2_N	R176	DNP	0R		
DSI_D3_P	R177	DNP	0R	LVDS/DSI_D3_P	3
LVDS_D3_P	R178	DNP	0R		
DSI_D3_N	R179	DNP	0R	LVDS/DSI_D3_N	3
LVDS_D3_N	R180	DNP	0R		

MIPI DSI LCD

MIPI CSI CAM

Parameter Set ClassName: USB_DIFF90
USB2

SMARC_USB1_N	R38	DNP	0R	DNP	
SMARC_USB3_N	R86	DNP	0R		
USBHUB_UP_D_N	R87	DNP	0R		
SMARC_USB1_P	R39	DNP	0R	DNP	
SMARC_USB3_P	R88	DNP	0R		
USBHUB_UP_D_P	R89	DNP	0R		

Parameter Set ClassName: USB_DIFF90
USB1

SMARC_USB0_N					
SMARC_USB0_P					
SMARC_USB0_VBUS_DET	R181		100K		
	R35		30K		
SMARC_USB0_OTG_ID_3V3	D3	RB521S30			

SMARC_USB3_VBUS_DET	R40		100K		
	R33	DNP	30K		
SMARC_USB3_OTG_ID	D2	DNP	RB521S30		
	R102	DNP	10K		
	R41		0R		

Parameter Set ClassName: USB_DIFF90

Parameter Set ClassName: CSI_DIFF100

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RONETIX DEVELOPMENT TOOLS

Ethernet

DESIGN NOTE:
If KSZ9031 is populated, then MODE0 should be 1.

DESIGN NOTE:
Default Ethernet strapping options:
PHYAD2-0: PHY address 0x1
MODE3-0: RGMII mode (10/100/1000 half/full duplex)
CLK125_EM: ref. clock disable
LED_MODE: Tri-color

Parameter Set
ClassName: ENET_RGMGII_TX
Matched Net Lengths [Tolerance = 250mil]
Length Constraint [Min Length = 0mil Max Length = 1750mil]

U9 KSZ9131RNXI

ENET1_TD0 19 TXD0
ENET1_TD1 20 TXD1
ENET1_TD2 21 TXD2
ENET1_TD3 22 TXD3
ENET1_TXC 24 TXC
ENET1_TX_CTL 25 TX_CTL

ENET1_RD0 R98 22R ENET1_RD0_R 32 RXD0/MODE0
ENET1_RD1 R99 22R ENET1_RD1_R 31 RXD1/MODE1
ENET1_RD2 R100 22R ENET1_RD2_R 28 RXD2/MODE2
ENET1_RD3 R110 22R ENET1_RD3_R 27 RXD3/MODE3
ENET1_RXC R111 22R ENET1_RXC_R 35 RXC/PHYAD2
ENET1_RX_CTL R112 22R ENET1_RX_CTL_R 33 RX_CTL/CLK125_EN

ETH1_ALLPHYAD 38 INT_N/PME_N2/ALLPHYAD
ETH1_LED_MODE 41 CLK125_NDO/LED_MODE

ENET1_MDC 36 MDC
ENET1_MDIO 37 MDIO
GPIO2_IO29 42 RESET_N

TP15 TP16 TP17
VDD_1V8 R119 2.2K

GND C109 18p/50V TP20
X32525MR84SI
GND Y5 GND
GND C117 18p/50V TP21

R117 6.04K ISET 6.04k

VDD_1V8
C114 100nF/10V
C115 100nF/10V
C116 100nF/10V
C118 22uF/6.3V

VDD_1V2
C122 100nF/10V
C124 100nF/10V
C126 100nF/10V
C127 100nF/10V
C128 100nF/10V
C129 100nF/10V

XI [50 ppm]
XO [Max 25pF]
-40° +85°C
Power Up
1.8V, 3.3V
1.2V
1.2V - 220mA max

TXD0 TXD1 TXD2 TXD3 TXC TX_CTL
RXD0/MODE0 RXD1/MODE1 RXD2/MODE2 RXD3/MODE3 RXC/PHYAD2 RX_CTL/CLK125_EN
INT_N/PME_N2/ALLPHYAD CLK125_NDO/LED_MODE
MDC MDIO RESET_N
XI XO ISET
DVDDH DVDDH DVDDH
NC(DVDDL) DVDDL DVDDL DVDDL DVDDL DVDDL
AVDDL AVDDL AVDDL_PLL LDO_O NC(VSS) VSS PGND
TXRXP_A TXRXM_A TXRXP_B TXRXM_B TXRXP_C TXRXM_C TXRXP_D TXRXM_D
LED2/PHYAD1 LED1/PME_N1/PHYAD0
AVDDH AVDDH NC(AVDDH)

ClassName: ETH
Net Class
DIFF100

GBE0_MDI0_P GBE0_MDI0_N
GBE0_MDI1_P GBE0_MDI1_N
GBE0_MDI2_P GBE0_MDI2_N
GBE0_MDI3_P GBE0_MDI3_N

DESIGN NOTE:
LED1 and LED2 are push-pull outputs

ETH1_LED2 15
ETH1_LED1 17

ETHERNET 1

VDD_1V8
R96 100K Q10 RU1C001UNTCL
Q11 RU1C001UNTCL
R94 0R GBE0_LINK1000#
R97 DNP 0R
GND

VDD_1V8
R116 100K Q12 RU1C001UNTCL
Q13 RU1C001UNTCL
R114 0R GBE0_LINK100#
R115 DNP 0R GBE0_LINK_ACT#
GND

ENET1_AVDDH 1 12 47
FB2 0603 120R/2A - BLM18PG121SN1D VDD_3V3
C113 22uF/6.3V
C110 C111 C112 100nF/10V
GND

ENET1_AVDDL 4 9
FB3 0603 120R/2A - BLM18PG121SN1D VDD_1V2
C119 4.7uF/6.3V
C120 C121 100nF/10V
GND

ENET1_AVDDL_PLL 44
FB4 0402 220R/0.45A - BLM15AG221SN1D VDD_1V2
max 7mA
C125 4.7uF/6.3V
C123 100nF/10V
GND

VDD_1V8
R118 DNP 10K
R120 DNP 10K
R121 R122 R123 R124 10K
ETH1_LED_MODE LED_MODE
ENET1_RD0_R MODE0
ENET1_RD1_R MODE1
ENET1_RD2_R MODE2
ENET1_RD3_R MODE3
ETH1_LED1 PHYAD0
ETH1_LED2 PHYAD1
ENET1_RXC_R PHYAD2
ENET1_RX_CTL_R CLK125_EN
R125 1K
R126 R127 R128 R129 1K
GND

VDD_1V8
R133 10K R134 10K
ETH1_ALLPHYAD
ETH2_ALLPHYAD

Parameter Set
ClassName: ENET_RGMGII_TX
Matched Net Lengths [Tolerance = 250mil]
Length Constraint [Min Length = 0mil Max Length = 1750mil]

U10 KSZ9131RNXI

ENET2_TD0 19 TXD0
ENET2_TD1 20 TXD1
ENET2_TD2 21 TXD2
ENET2_TD3 22 TXD3
ENET2_TXC 24 TXC
ENET2_TX_CTL 25 TX_CTL

ENET2_RD0 R135 22R ENET2_RD0_R 32 RXD0/MODE0
ENET2_RD1 R136 22R ENET2_RD1_R 31 RXD1/MODE1
ENET2_RD2 R137 22R ENET2_RD2_R 28 RXD2/MODE2
ENET2_RD3 R139 22R ENET2_RD3_R 27 RXD3/MODE3
ENET2_RXC R140 22R ENET2_RXC_R 35 RXC/PHYAD2
ENET2_RX_CTL R142 22R ENET2_RX_CTL_R 33 RX_CTL/CLK125_EN

ETH2_ALLPHYAD 38 INT_N/PME_N2/ALLPHYAD
ETH2_LED_MODE 41 CLK125_NDO/LED_MODE

VDD_1V8 R151 2.2K
ENET2_MDC 36 MDC
ENET2_MDIO 37 MDIO
GPIO2_IO29 42 RESET_N

TP18 TP19 TP22
GND C130 18p/50V
X32525MR84SI
GND Y6 GND
GND C138 18p/50V TP23

R148 6.04K ISET 6.04k

VDD_1V8
C135 100nF/10V
C136 100nF/10V
C137 100nF/10V
C139 22uF/6.3V

VDD_1V2
C143 100nF/10V
C145 100nF/10V
C147 100nF/10V
C148 100nF/10V
C149 100nF/10V
C150 100nF/10V

XI [50 ppm]
XO [Max 25pF]
-40° +85°C
Power Up
1.8V, 3.3V
1.2V
1.2V - 220mA max

TXD0 TXD1 TXD2 TXD3 TXC TX_CTL
RXD0/MODE0 RXD1/MODE1 RXD2/MODE2 RXD3/MODE3 RXC/PHYAD2 RX_CTL/CLK125_EN
INT_N/PME_N2/ALLPHYAD CLK125_NDO/LED_MODE
MDC MDIO RESET_N
XI XO ISET
DVDDH DVDDH DVDDH
NC(DVDDL) DVDDL DVDDL DVDDL DVDDL DVDDL
AVDDL AVDDL AVDDL_PLL LDO_O NC(VSS) VSS PGND
TXRXP_A TXRXM_A TXRXP_B TXRXM_B TXRXP_C TXRXM_C TXRXP_D TXRXM_D
LED2/PHYAD1 LED1/PME_N1/PHYAD0
AVDDH AVDDH NC(AVDDH)

ClassName: ETH
Net Class
DIFF100

GBE1_MDI0_P GBE1_MDI0_N
GBE1_MDI1_P GBE1_MDI1_N
GBE1_MDI2_P GBE1_MDI2_N
GBE1_MDI3_P GBE1_MDI3_N

ETH2_LED2 15
ETH2_LED1 17

ETHERNET 2

VDD_1V8
R131 100K Q6 RU1C001UNTCL
Q7 RU1C001UNTCL
R130 0R GBE1_LINK1000#
R132 DNP 0R
GND

VDD_1V8
R143 100K Q14 RU1C001UNTCL
Q15 RU1C001UNTCL
R138 0R GBE1_LINK100#
R141 DNP 0R GBE1_LINK_ACT#
GND

ENET2_AVDDH 1 12 47
FB5 0603 120R/2A - BLM18PG121SN1D VDD_3V3
C131 22uF/6.3V
C132 C133 C134 100nF/10V
GND

ENET2_AVDDL 4 9
FB6 0603 120R/2A - BLM18PG121SN1D VDD_1V2
C140 4.7uF/6.3V
C141 C142 100nF/10V
GND

ENET2_AVDDL_PLL 44
FB7 0402 220R/0.45A - BLM15AG221SN1D VDD_1V2
max 7mA
C146 4.7uF/6.3V
C144 100nF/10V
GND

VDD_1V8
DNP R150 10K
R152 DNP 10K
R153 R154 R155 10K
R149 10K
ETH2_LED_MODE LED_MODE
ENET2_RD0_R MODE0
ENET2_RD1_R MODE1
ENET2_RD2_R MODE2
ENET2_RD3_R MODE3
ETH2_LED1 PHYAD0
ETH2_LED2 PHYAD1
ENET2_RXC_R PHYAD2
ENET2_RX_CTL_R CLK125_EN
R156 1K
R157 R158 R159 R160 1K
GND

VDD_1V8
R145 10K R146 10K
ETH1_ALLPHYAD
ETH2_ALLPHYAD

DESIGN NOTE:
Default Ethernet strapping options:
PHYAD2-0: PHY address 0x2
MODE3-0: RGMII mode (10/100/1000 half/full duplex)
CLK125_EM: ref. clock disable
LED_MODE: Tri-color

RGMII Routing Constraints (Reduced Gigabit Media Independent Interface):

The RGMII signals must be length-matched by TX and RX groups.
That is, the TX group should be matched within 0.25 inch (6.35 mm), and the RX group should be matched within 0.25 inch (6.35 mm). Total length should not exceed 1.75 inch (44.5 mm). There is no requirement to match the TX and RX groups because their clocks are not related.

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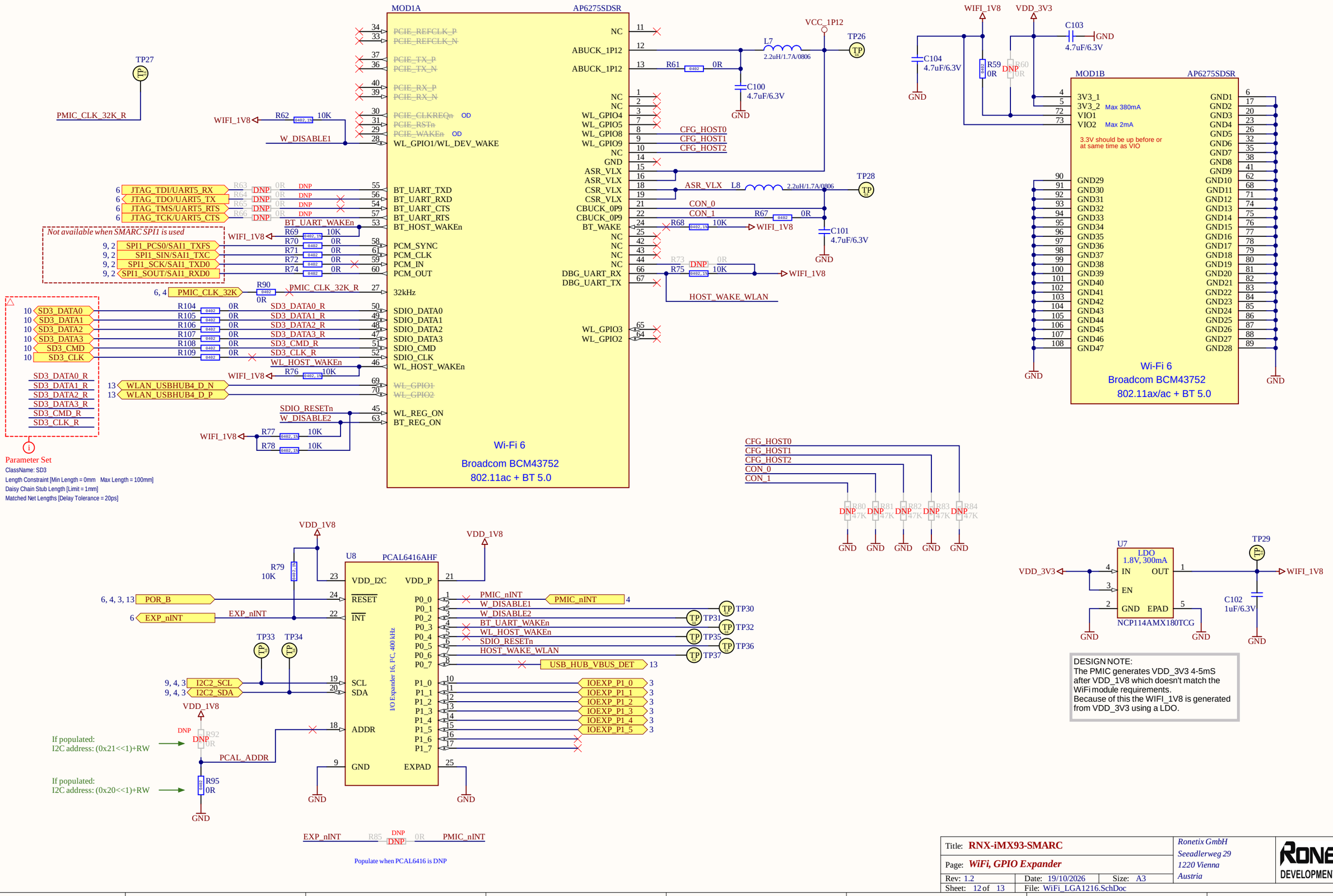
RONETIX DEVELOPMENT TOOLS

WiFi, GPIO Expander



Title: **RNX-iMX93-SMARC**			*Ronetix GmbH*
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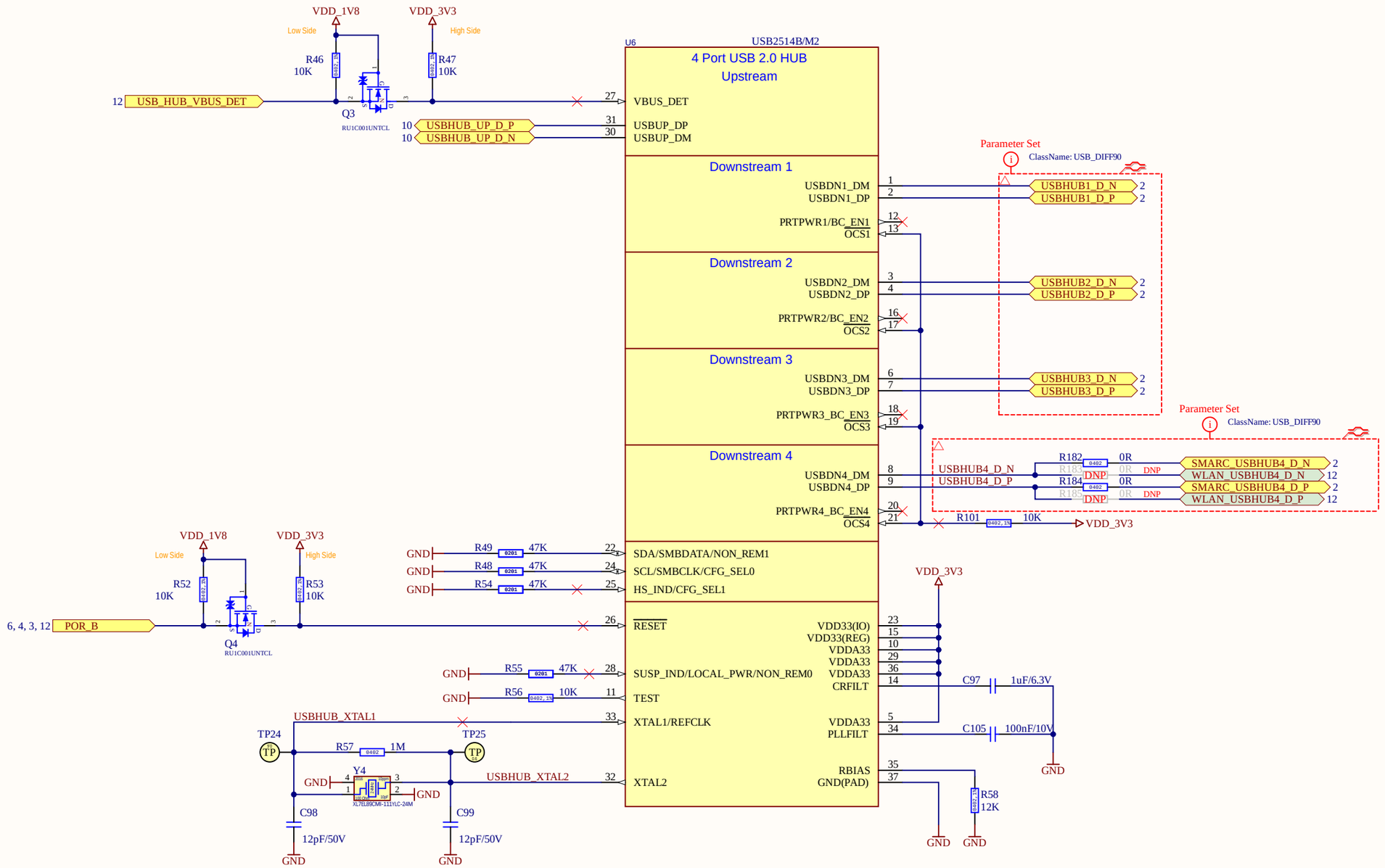
4 Port USB 2.0 Hub



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